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FUJITSU

DATA SHEET

MB86468

AUDIO FILTER FOR ANALOG CORDLESS TELEPHONE

Audio Filter for Analog Cordless Telephone With Compandor, 2400 Bps MSK Modem, Speech Scrambler

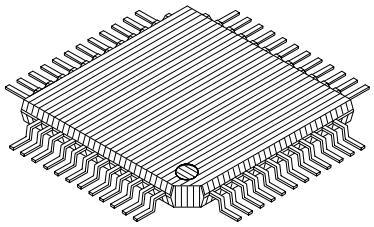
The MB86467 is a single-chip voice filter which contains a 2400-bps minimum shift keying (MSK) modem, speech scrambler, and compandor for cordless telephones.

The MSK modem incorporates a frame-signal detection function.

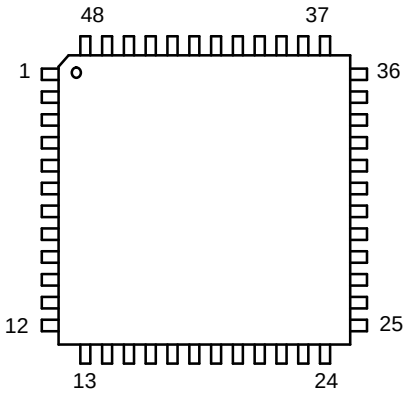
The transmitter consists of a transmitting amplifier, compressor, speech scrambler, mute function, limiter, and splatter filter. The receiver consists of a receiving amplifier, expander, speech scrambler, and a mute function. Both the transmitter and receiver use switched capacitor filter (SCF) technology.

The MB86468 can operate at low voltages of 2.7 V min. and is ideally suitable for analog cordless telephones.

48-Pin Plastic QFP
(FPT-48P-M02)



(TOP VIEW)



(FPT-48P-M02)

FEATURES

- **Transmission/reception filter:**
  - CMOS compandor:
    I/O compression ratio of 1/2 logarithm
    I/O expansion ratio of 2 algorithm
  - Built-in speech scrambler
  - Transmitter with limiter:
    Externally-controllable limiter level
    Limiter non-operation settable for modem use
  - Muting function in transmitter and receiver
  - Input gain adjustment amplifiers in transmitter and receiver
  - Electronic gain-controls in transmitter and receiver: +9.8 to –11.2 dB, 1.4 dB step control
- **2400-bps MSK modem:**
  - Full-duplex operation
  - Frame signal detection function; 16/20 bit selectable
  - Controllable receive clock and data output after frame signal detection
  - Selectable hysteresis input
  - Selectable frame synchronization patterns (for base and portable units)
- **Digital Circuit:**
  - Serial interface: Interfacing via signal line with smaller number of lines
  - Crystal oscillator circuit: 3.6864 MHz oscillation frequency
  - Six standby modes for optimum low power consumption
  - CMOS I/O level interfacing
- **Power supply voltage: 2.7 to 5.5 V**
- **Operating temperature: –30° to +70°C**
- **48-pin plastic QFP package**

Caution
This device should not be used in restricted applications such as in wiretapping or eavesdropping.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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PIN ASSIGNMENT

Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol
1	I	CC_2	13	I	DEM_1	25	I	D_{IN}	37	O	OSC_{OUT}
2	O	CC_1	14	O	DEM_2	26	I	DSTB	38	I	OSC_{IN}
3	I	SCR_{IN}	15	O	CC_3	27	I	DCK	39	I	RST
4	O	CMP_{OUT}	16	I	CC_4	28	I	FCL	40	O	$TAMP_{OUT}$
5	O	CAP-C	17	O	DSC_{OUT}	29	O	FD_{OUT}	41	I	$TAMP_{IN}$
6	—	A.GND	18	I	EXP_{IN}	30	—	D.GND	42	O	MOD
7	O	AF_{IN2}	19	—	V_{DDA}	31	O	RCK	43	—	V_{DDD}
8	I	AF_{IN1}	20	O	CAP-E	32	O	RD	44	I	LIM_{IN}
9	I	1/2 V_{DDIN}	21	O	AF_{OUT}	33	O	LOCK	45	O	$SAMP_{OUT}$
10	O	1/2 V_{DDOUT}	22	I	$RAMP_{IN}$	34	I	SD	46	I	$SAMP_{IN}$
11	O	CC_5	23	O	$RAMP_{OUT}$	35	O	SCK	47	O	S_{OUT}
12	I	CC_6	24	I	TEST	36	I	SEND	48	O	EMP_{OUT}

PIN DESCRIPTION

Block function	Pin No.	Symbol	I/O	Name	Description
Transmit filter block	8	AF_{IN1}	I	Input-amplifier inverted-signal input pin	Form an input filter by providing external resistors R1, R2 and R3 and external capacitors C1 and C2 at the AF_{IN1} and AF_{IN2} pins.
	7	AF_{IN2}	O	Input-amplifier output pin	
	5	CAP-C	O	Compressor AC-cutoff capacitor pin	Determine the cutoff frequency of the low band by multiplying the capacitance of the external capacitor by the internal resistance of 220 kΩ.
	4	CMP_{OUT}	O	Compressor output pin	—
	3	SCR_{IN}	I	Scrambler input pin	Inputs signal output from compressor to scrambler, while cutting off direct current
	1	CC_2	I	Scrambler capacitor pin	Insert a 0.047 μF DC-cutoff capacitor between the CC_1 and CC_2 pins.
	2	CC_1	O		
	48	EMP_{OUT}	O	Scrambler output pin	Outputs scrambled transmit signal
	47	S_{OUT}	O	Modulator output pin	Outputs MSK modulated signal
	46	$SAMP_{IN}$	I	Inverted-signal input pin for limiter input-amplifier	Inputs inverted-signal to added transmitter amplifier
	45	$SAMP_{OUT}$	O	Limiter input-amplifier output pin	Outputs signal from added transmitter amplifier
	44	LIM_{IN}	I	Limiter level input pin	When this pin is open, the limiter output level range is set to $0.05 \times V_{DD}$. When the voltage V_{LIM} ranges from 0 to 1/2 $V_{DD} - 0.04 \times V_{DD}$ is applied at LIM_{IN} pin, the limiter output level range is limited to $V_{DD} - V_{LIN}$ to V_{LIM}.
	41	$TAMP_{IN}$	I	Inverted-signal input pin for output-gain adjustment amplifier	Adjust the output gain of the transmit block by connecting external resistors R10 and R11 to the $TAMP_{IN}$, MOD, and $TAMP_{OUT}$ pins.
	40	$TAMP_{OUT}$	O	Output-gain adjustment amplifier output pin	
	42	MOD	O	Transmit filter block output pin	—

(Continued)

Block function	Pin No.	Symbol	I/O	Name	Description
Receiver filter	13	DEM_1	I	Input-amplifier inverted-signal input pin	Form an input amplifier by providing external resistors R4 and R6 at the DEM_1 and DEM_2 pins. The gain may be adjusted by adjusting the resistance of the external resistors.
	14	DEM_2	O	Input-amplifier output pin	
	15	CC_3	O	Descrambler capacitor pin	Insert a 0.47 µF DC-cutoff capacitor between the CC_3 and CC_4 pins.
	16	CC_4	I		
	17	DSC_{OUT}	O	Descrambler output pin	—
	18	EXP_{IN}	I	Internal expander input pin	—
	20	CAP-E	O	Expander AC-cutoff capacitor pin	Determine the cutoff frequency of the low band by multiplying the capacitance of the external capacitor by the internal resistance of 220 kΩ.
	21	AF_{OUT}	O	Expander output pin	—
	22	$RAMP_{IN}$	I	Inverted-signal output pin for added receiver-amplifier	—
	23	$RAMP_{OUT}$	O	Added receiver-amplifier output pin	Outputs from receiver
Digital section	38	OSC_{IN}	I	Crystal oscillator input/output pins	Insert a 3.6864-MHz crystal oscillator between the OSC_{IN} and OSC_{OUT} pins.
	37	OSC_{OUT}	O		
	39	RST*	I	Reset signal input pin	When this pin is set to L, all circuits are reset.
	24	TEST*	I	Test input pin	This pin should be open or set to H.
	25	D_{IN}	I	Serial signal input pin	Input a serial interface signal.
	26	DSTB	I	Serial signal input strobe pin	A serial signal is transferred to the mode-selection register via the D_{IN} pin at the rise of the DSTB signal. Set this pin to H level during data input.
	27	DCK	I	Serial signal input clock pin	The serial input signal (D_{IN}) is synchronous with the rising edge of this clock input (DCK)

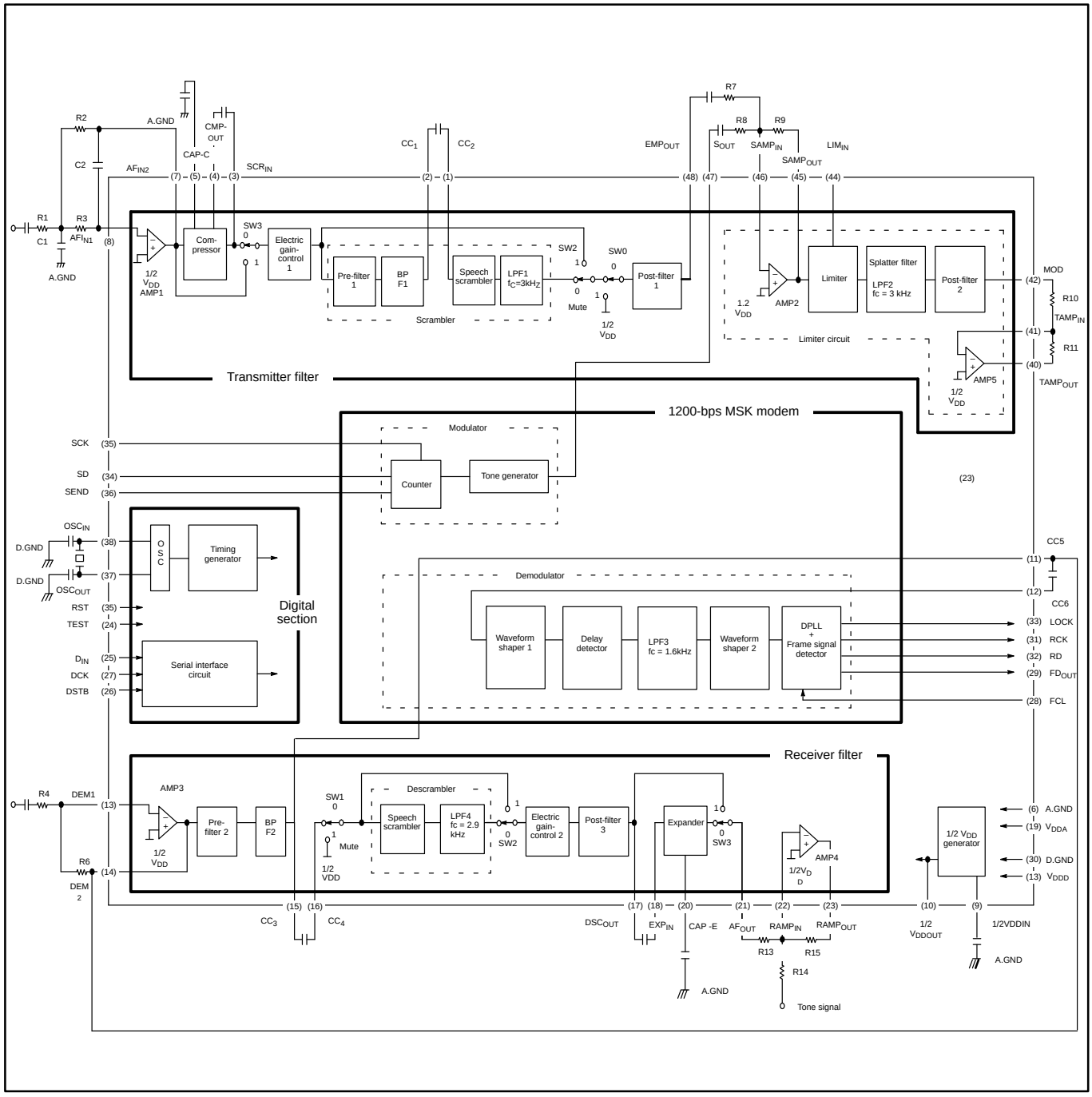
*High-resistance pull-up pin

(Continued)

Block function	Pin No.	Symbol	I/O	Name	Description
MSK modem block	35	SCK	O	MSK modem transmitter clock output pin	Inputs SD data synchronized with the rising edge of SCK signal
	34	SD	I	MSK modem transmitter data input pin	—
	36	SEND	I	MSK modem transmitter mute pin	"H" level: SCK pin outputs MSK signal. S_{OUT} pin outputs modulated signal. "L" level: SCK pin fixed to "H". S_{OUT} pin outputs no signal.
	11	CO_5	O	Demodulator capacitor pin	This pin should be left open. (Pin 11) Insert a 0.47 µF DC-cutoff capacitor between the DEM_2 and CO_6 pins.
	12	CO_6	I		
	33	LOCK	O	Lock signal output pin	When the DPLL signal is within 1/4 clock cycle of the RCK signal, this pin changes from "H" to "L" level.
	31	RCK	O	MSK modem receiver clock output pin	Outputs RD data at rising edge of clock from RCK pin
	32	RD	O	MSK modem receiver data output pin	—
	29	FD_{OUT}	O	Frame detector output signal pin	After reset is cancelled, the FD_{OUT} pin becomes "H" level when the RD pin outputs a code according to the frame synchronization pattern.
	28	FCL*	I	Frame detection latch clear pin	The FD_{OUT} pin is set to "L" when this pin is "L" level. Always set the FCL pin to "L" level after setting a frame synchronization pattern, except at resetting.
Power supply block	19	V_{DDA}	—	Analog power supply pin	Input the same supply voltage to the V_{DDA} and V_{DDD} pins in the range of 2.7 to 5.5 V.
	43	V_{DDD}	—	Digital power supply pin	
	6	A.GND	—	Analog ground pin	—
	30	D.GND	—	Digital ground pin	—
	9	1/2 V_{DDIN}	I	1/2 V_{DD} generator input pin	Insert a 1 µF bypass capacitor between the 1/2 V_{DDIN} and A.GND pins.
	10	1/2 V_{DDOUT}	O	1/2 V_{DD} generator output pin	Internal circuits operate at a reference voltage of 1/2 V_{DDOUT}.

*High-resistance pull-up pin

BLOCK DIAGRAM



BLOCK FUNCTIONS

The MB86467 consists of a transmitter filter, receiver filter, MSK modem, and digital section. The transmitter has a speech-scrambler and compressor. The receiver has a speech-scrambler and expander.

1. Transmitter Filter

1.1 Input filter

A voice signal input via the AF_{IN1} pin is sent to the compressor after being band-limited by the input amplifier formed with AMP1 and external resistors R1, R2, and R3 and the external capacitors C1 and C2.

1.2 Compressor

The voice signal from the input filter is sent to the scrambler via the electronic gain-control 1 after being compressed to half logarithmically by the compressor.

Bypass of the compressor may be controlled via the serial input D_{IN} and adjustment of the volume of the transmitted voice by the electronic gain-control 1.

1.3 Scrambler

The compressed signal from the compressor is output as a scrambled signal via the EMP_{OUT} pin after passing the prefilter 1, BPF1, external capacitor, scrambler, LPF1, and post filter.

Bypass of the scrambler and muting of the output voice may be controlled via the serial input D_{IN}.

1.4 Limiter

The output signals from the EMP_{OUT} and S_{OUT} pins are input to the adding amplifier AMP2 via the $SAMP_{IN}$ pin after passing the external RC circuit. The limit level of the signal output from limitter can be adjusted by the input level at the LIM_{IN} pin.

The voice signal is limited to 3 kHz by the splatter filter LPF2 and output via the MOD pin after passing the post-filter 2. The output gain of the voice signal can be adjusted by the AMP5 and external resistors R10 and R11.

2. Receiver Filter

2.1 Input filter

A voice signal received via the DEM_1 pin is band-limited by the pre-filter 2 and BPF2 after passing an inverting amplifier that consists of the input amplifier AMP3 and external resistors R4 and R5. The input gain of the voice signal can be controlled by this inverting amplifier.

Muting of the input voice signal may be controlled via the serial input D_{IN}.

2.2 Descrambler

The voice signal from BPF2 is output via the DSC_{OUT} pin after passing the external capacitors, descrambler, LPF4, electronic gain-control 2, and post-filter 3. Bypass of the descrambler may be controlled via the serial input D_{IN} and adjustment of the volume of the received voice by the electronic gain-control 2.

2.3 Expander

The voice signal from the descrambler is input to the expander via the EXP_{IN} pin after passing the external capacitors. The signal is doubled logarithmically and then output via the AF_{OUT} pin. The received voice signal from the AF_{OUT} pin is output as a voice signal via $RAMP_{OUT}$ after being synthesized with a tone signal by the adding amplifier AMP4.

Bypass of the expander may be controlled via the serial input D_{IN}.

3. MSK Modem Block

3.1 MSK modulator

This modulator outputs a 1200- or 2400-Hz sine-wave signal corresponding to the respective data “1” or “0” input via the SD pin, which is synchronized with the transmission clock signal (SCK).

AMP2 synthesizes this output signal with the transmitting voice signal.

3.2 MSK demodulator

A voice signal received via the DEM_1 pin is sent to the demodulator (CC_6) after passing the input-gain amplifier AMP3. The voice (analog) signal is digitized by the waveform shaper 1 and reproduced by the delay detector. The reproduced data is reconverted to a digital signal after noise components are eliminated by LPF3.

The DPLL circuit generates and outputs a receive clock signal synchronized with the reproduced data via the RCK pin; it outputs the reproduced data via the RD pin. This circuit also incorporates a frame-signal detection function and outputs a High level signal via the FD_{OUT} pin when the reproduced output data from the RD pin matches the frame synchronization pattern.

Selection of the frame synchronization pattern for the base and portable units may be controlled via the serial input D_{IN}. The RCK and RD outputs can be held at Low level until frame detection is completed.

4. Digital Section

4.1 Timing generator

The timing generator generates a basic clock signal from an external crystal oscillator (3.6864 MHz) and internal crystal oscillator circuit. It sends a divided clock signal of the basic clock signal to the MSK modulator, MSK demodulator, and transmitter and receiver filters.

4.2 Serial interface circuit

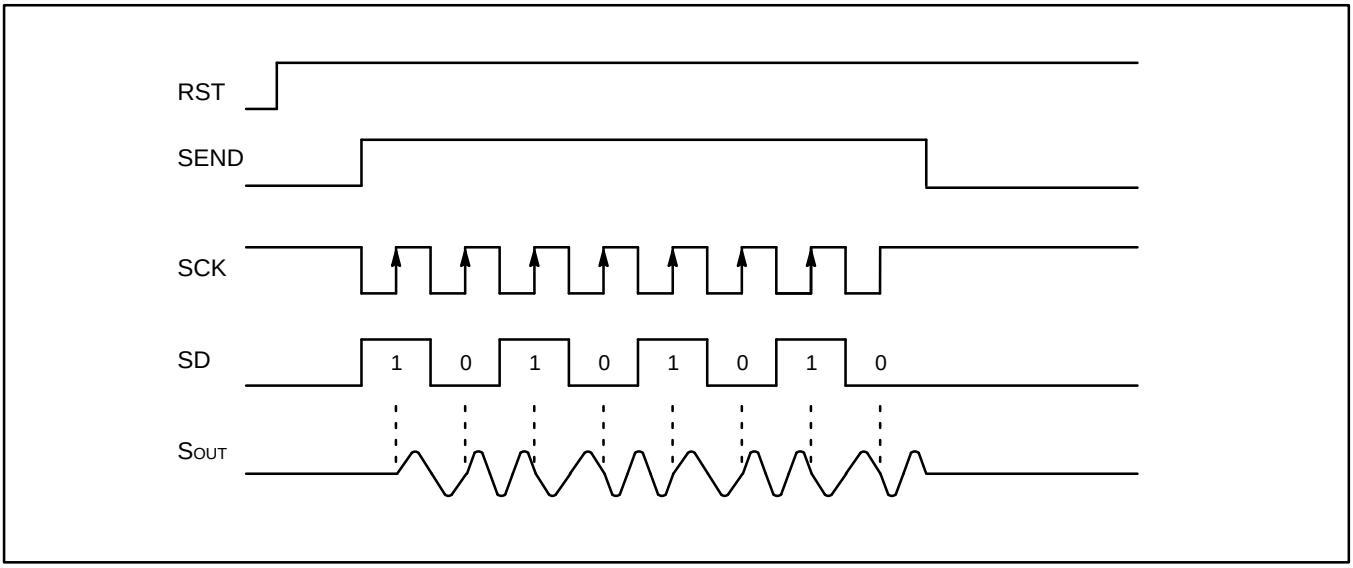
Inputting a serial signal to the serial interface circuit via the serial signal line (D_{IN}), clock signal line (DCK), and strobe signal line (DSTB) enables setting of various modes: Standby and bypass modes, ON/OFF of transmitter/receiver mute function, and the frame synchronization pattern. A microprocessor may be used to generate a serial input signal for the digital circuit.

OPERATION SEQUENCES

1. MSK Modem Operation Timing

1.1 Modulation timing

- When the SEND pin is High level, at the rising edge of the SCK clock, the S_{OUT} pin outputs:
  - 1200 Hz sine-wave signals when the SD pin is High level
  - 2400 Hz sine-wave signals when the SD pin is Low level
- When the SEND pin is Low level, the SCK pin is kept at High level and the SD pin is kept at Low level.

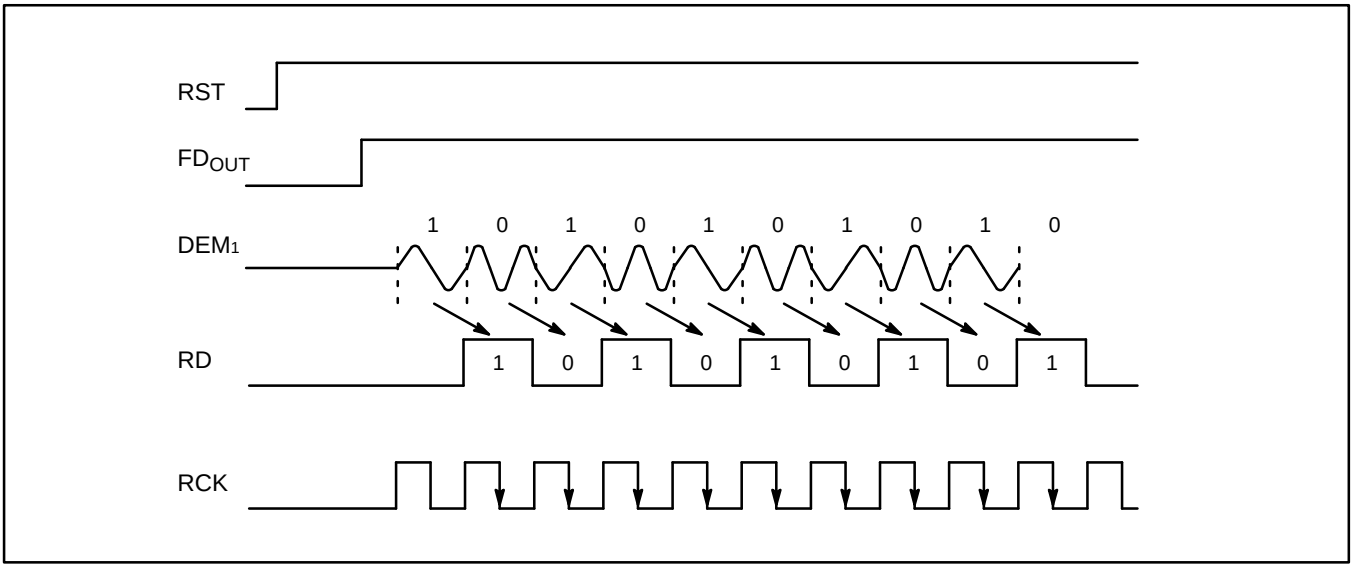


1.2 Demodulation timing

When the FD_{OUT} pin is High level, at the rising edge of the RCK clock, the RD pin outputs:

- "1" signal when the DEM_1 pin receives 1200 Hz signals
- "0" signal when the DEM_1 pin receives 2400 Hz signals

RD output data should be entered to a microcontroller at the falling edge of the RCK clock.



1.3 Frame detection timing (D8 = 0)

The 5th bit (D5) of a serial signal input via the D_{IN} pin determines the frame detection bit pattern.

- Bit pattern from base to portable units (D5 = “0”)

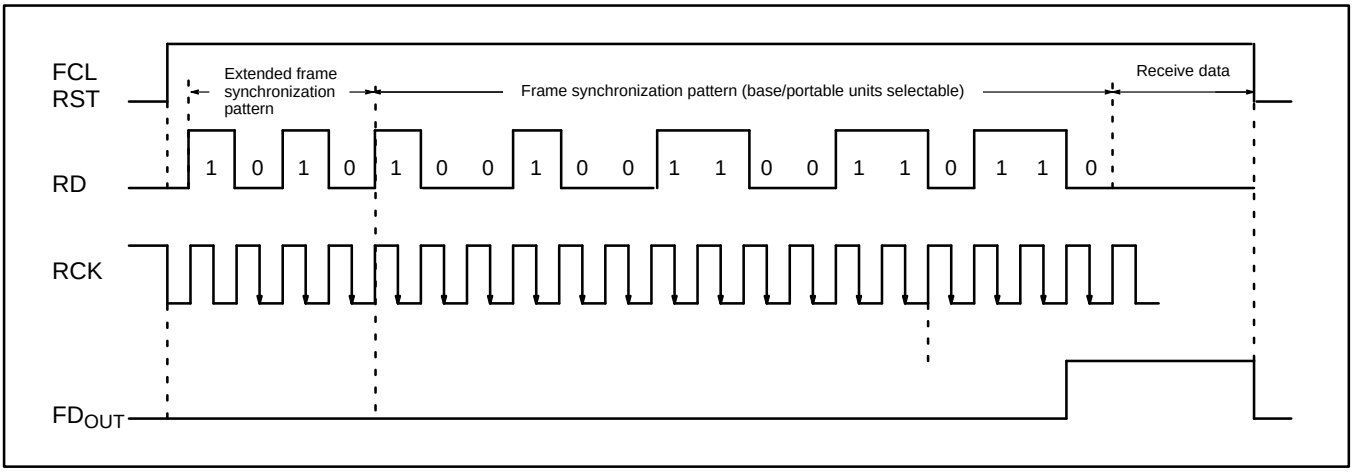
  “(1010) 1001 0011 0011 0110”

- Bit pattern from portable to base units (D5 = “1”)

  “(1010) 1100 0100 1101 0110”

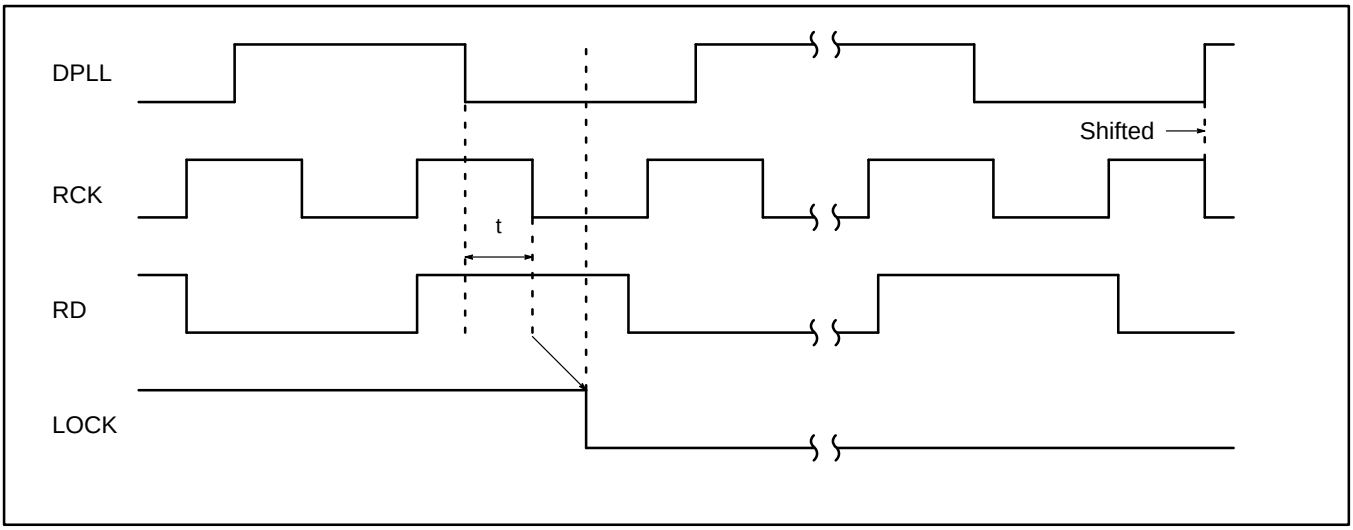
  ( ): Synchronization pattern for extended frame mode

Notes:
1. When the D_{IN} pin input serial signal D8 is “0” and D10 is “1”, setting the FD_{OUT} pin to Low level enables holding of the RD and RCK pins at Low level.
2. After setting the frame pattern, set the FCL pin to Low level and then the FD_{OUT} pin to Low level.



1.4 DPLL pulse shift timing

Shift the falling edge of the DPLL pulse near the falling edge of the RCK pulse so that the time lag (*t*) between them disappears. In this case, when the lag approaches 1/4 of the RCK pulse cycle, the LOCK pin changes to Low level.



2. Limiter Output Level

2.1 Limits of output level when LIM_{IN} pin open

LIM_{IN} Pin Input Level	$SAMP_{OUT}$ Pin Input Level	Output Level	Remarks
LIM_{IN} pin = open V_{DD} = 3.0 V	$V_I > \frac{V_{DD}}{2} + 0.15$	$\frac{V_{DD}}{2} + 0.15$	Max.
	$\frac{V_{DD}}{2} + 0.15 \geq V_I \geq \frac{V_{DD}}{2} - 0.15$	V_I	
	$\frac{V_{DD}}{2} - 0.15 > V_I$	$\frac{V_{DD}}{2} - 0.15$	Min.

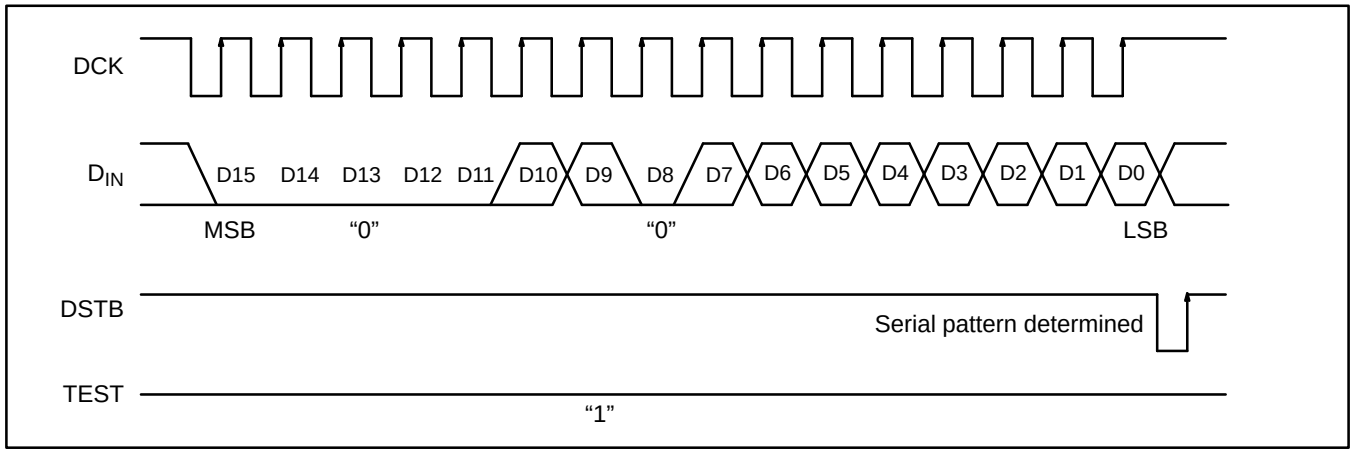
2.2 Limits of output level when LIM_{IN} pin = V_{LIM}

LIM_{IN} Pin Input Level	$SAMP_{OUT}$ Pin Input Level	Output Level	Remarks
LIM_{IN} pin = V_{LIM} (Adjust the input voltage for the LIM_{IN} pin to within 0 to 1/2 V_{DD} – 0.04 V_{DD}.)	$V_I > V_{DD} - V_{LIM}$	$V_{DD} - V_{LIM}$	Max.
	$V_{DD} - V_{LIM} \geq V_I \geq V_{LIM}$	V_I	
	$V_{LIM} > V_I$	V_{LIM}	Min.

3. Serial Interface Circuit

3.1 Operating mode selection by serial signal

- **Input condition of serial signal**



Note: A serial signal is input at the rising edge of the DCK clock pulse via the D_{IN} pin.

- **Bit codes for mode selection***

Bit No.	Functions	Code and Functions		Remarks
		“0”	“1”	
D2, D1, D0	Standby mode selection	“101” to “000”		See page 14.
D3	Transmission mute mode selection	Normal	Muted	Selection of SW0 on/off
D4	Reception mute mode selection	Normal	Muted	Selection of SW1 on/off
D5	Base/portable unit selection	Portable unit	Base unit	Output bit pattern of RD pin for frame detection • From base to portable units (D5 = “0”): “1001 0011 0011 0110” • From portable to base units (D5 = “1”): “1100 0100 1101 0110”
D6	Speech scramble mode selection	Operated	Bypassed	Selection of SW2 on/off
D7	Compandor mode selection	Operated	Bypassed	Selection of SW3 on/off
D8	Electronic gain-control adjustment	—	Set	Set to “0”.
D9	Hysteresis characteristic selection for waveform shaper 1	Not selected	Selected	Hysteresis (±20 mV) can be selected for input to waveform shaper 1.
D10	Demodulator output selection	Normal	After detection	A signal is output from the RD and RCK pins after frame detection. These pins are set to “L” level in operation.
D15 to D11	For test mode	Fixed	—	Set all bits to “0”.

*Bit pattern for reset (Input pattern to D_{IN} pin.)
D15 to D0: “0000 0000 0000 0100”

• **Standby mode selection table**

Block		Standby mode / Bit code / Circuit name		M0	M1	M2	M3	M4*	M5
				(D2, D1, D0) 0 0 0	(D2, D1, D0) 0 0 1	(D2, D1, D0) 0 1 0	(D2, D1, D0) 0 1 1	(D2, D1, D0) 1 0 0	(D2, D1, D0) 1 0 1
Transmitter	Voice filter	AMP1		×	×	○	○	○	○
		Compressor		×	×	○	○	○	○
		Electronic gain-control 1		×	×	○	○	○	○
		Transmission scrambler	Pre-filter 1 BPF1 LPF1	×	×	○	○	○	○
		Post-filter 1		×	×	○	○	○	○
		AMP2, Limiter, LPF2, Post-filter 2		×	×	○	○	○	○
		AMP5		×	×	○	○	○	○
	Modem	Modulator		×	○	○	○	○	○
		SCK output **		×	Fixed	×	×	×	○
Receiver	Voice filter	AMP3		×	×	×	×	○	○
		Pre-filter 2		×	×	×	×	○	○
		BFP2		×	×	×	○	○	○
		Reception scrambler	LPF4 Electronic gain-control 2 Post-filter 3	×	×	×	○	○	○
		Expander		×	×	×	○	○	○
		AMP4		×	×	×	○	○	○
	Modem	Demodulator	LPF3 Waveform shaper 1	×	×	×	×	○	○
Others		OSC		×	×	×	×	×	○
		1/2 V_{DD} generator		×	×	×	×	○	○

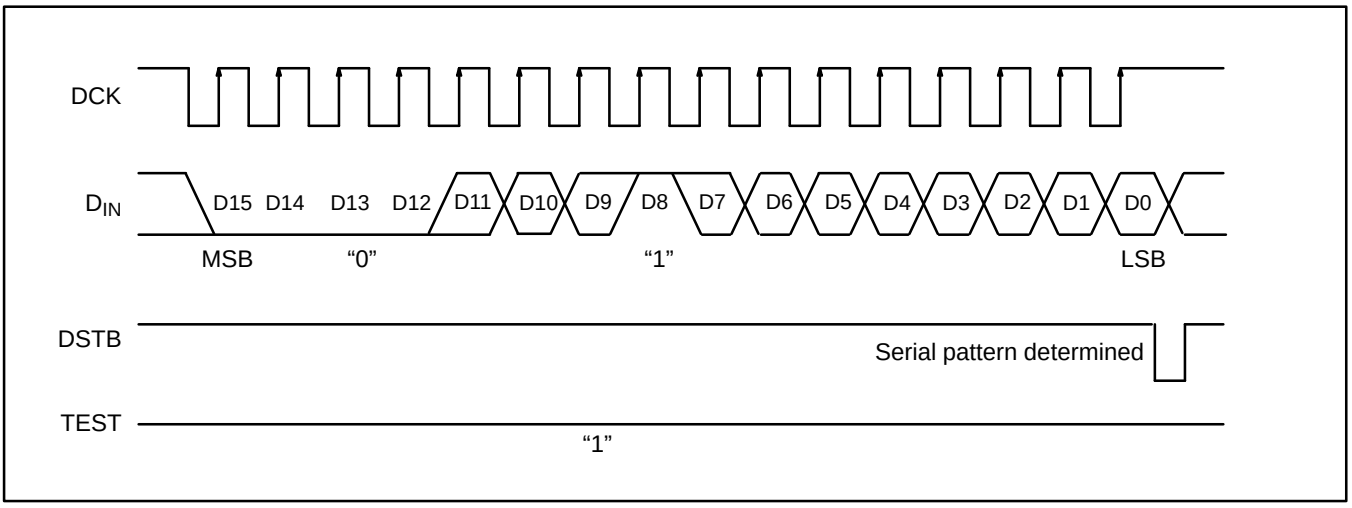
× : Active ○ : Inactive

*Mode M4 is for resetting.

**In modes M_1 and M_5, or when SEND is “L” level, the SCK is kept High level.

3.2 Electronic gain-control adjustment by serial signal

- **Input conditions of serial signal**



Note: A serial signal is input at the rising edge of the DCK clock pulse via the D_{IN} pin.

- **Bit codes for mode selection***

Bit No.	Functions	Code and Functions		Remarks
		0	1	
D0 to D3	Setting of electronic gain-control 1	1111 to 0000		See page 16.
D4 to D7	Setting of electronic gain-control 2	1111 to 0000		
D8	Electronic gain-control adjustment	—	Set	Set to 1.
D9	Scrambler clock selection	Normal mode	Selected mode	Normal mode: 3.388 kHz Selected mode: 3.285 kHz
D10	Expanded frame detection	16 bits	20 bits	Output bit pattern of RD pin for expanded frame detection • From base to portable units - D10 = "1": "1010 1001 0011 0011 0110" (20 bits) - D10 = "0": "1001 0011 0011 0110" (16 bits) • From portable to base units - D10 = "1": "1010 1100 0100 1101 0110" (20 bits) - D10 = "0": "1100 0100 1101 0110" (16 bits)
D11	Limiter control	limited	No limit	SEND pin = "1"**
		Limited		SEND pin = "0"
D12 to D15	Unused bits	Fixed	—	Set all bits to "0".

*Bit pattern for reset (Input pattern to D_{IN} pin.)
D15 to D0: 0000 0001 1001 1011
**When D11 is "1", limiter control does not function irrespective of the voltage of the LIM pin.

- **Set code for electronic gain-control output gain**

	Set Bits				
Electronic Gain-Control 1	**D7**	**D6**	**D5**	**D4**	**Output gain (dB)**
Electronic Gain-Control 2	**D3**	**D2**	**D1**	**D0**	
Set Code	1	1	1	1	9.8
	1	1	1	0	8.4
	1	1	0	1	7.0
	1	1	0	0	5.6
	1	0	1	1	4.2*
	1	0	1	0	2.8
	1	0	0	1	1.4**
	1	0	0	0	0.0
	0	1	1	1	–1.4
	0	1	1	0	–2.8
	0	1	0	1	–4.2
	0	1	0	0	–5.6
	0	0	1	1	–7.0
	0	0	1	0	–8.4
	0	0	0	1	–9.8
	0	0	0	0	–11.4

*Reset condition: Electronic gain-control 1 = “1011”

**Reset condition: Electronic gain-control 2 = “1001”

Compandor

1. Electrical Characteristics

1.1 Compressor

- **Reference input voltage (0 dBm0): –20 +20 log (V_{DD}/3 V) [dBV]**
- **Output voltage at 0 dBmo input: –20 +20 log (V_{DD}/3 V) [dBV]**
- **Compression characteristics**

Input Voltage Limits	Compression Ratio
$V_{IN} \geq$ 20 dBmo	$\Delta V_{OUT}/\Delta V_{IN}$ = 1
20 dBmo > $V_{IN} \geq$ –50 dBmo	$\Delta V_{OUT}/\Delta V_{IN}$ = 1/2
–50 dBmo > V_{IN}	$\Delta V_{OUT}/\Delta V_{IN}$ = 1

1.2 Expander

- **Reference input voltage (0 dBm0): –14 +20 log (V_{DD}/3 V) [dBV]**
- **Output voltage at 0 dBmo input: –14 +20 log (V_{DD}/3 V) [dBV]**
- **Expansion characteristics**

Input Voltage Limits	Compression Ratio
$V_{OUT} \geq$ 10 dBmo	$\Delta V_{OUT}/\Delta V_{IN}$ = 1
10 dBmo > $V_{OUT} \geq$ –70 dBmo	$\Delta V_{OUT}/\Delta V_{IN}$ = 2
–70 dBmo > V_{OUT}	$\Delta V_{OUT}/\Delta V_{IN}$ = 1

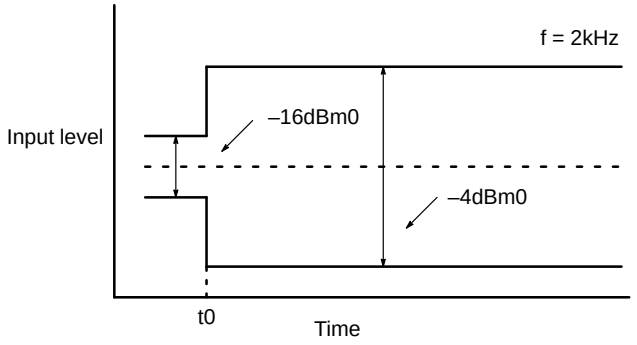
2. Attack and Recovery Time Test Method

2.1 Compressor

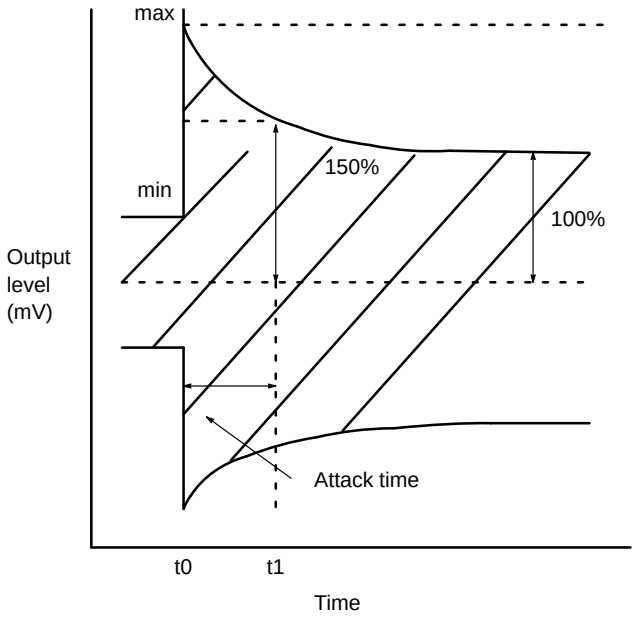
a. Attack time

- **Input conditions***

*When the reference input level to the compressor is 0 dBm0, the input level is as follows:



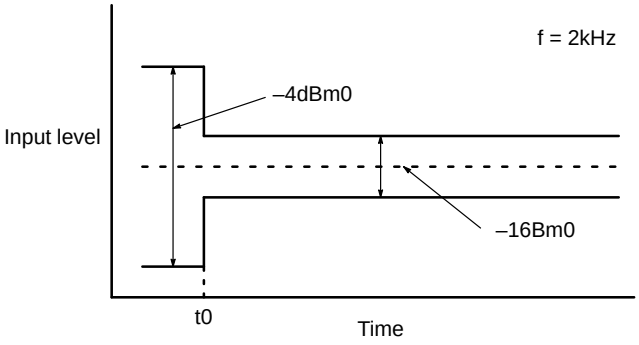
- **Output transient response characteristics**



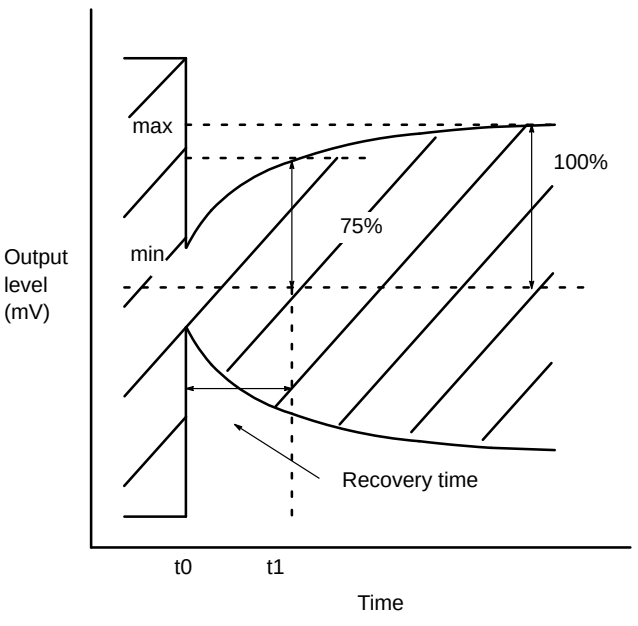
b. Recovery time

- **Input conditions***

*When the reference input level to the compressor is 0 dBm0, the input level is as follows:



- **Output transient response characteristics**



Note: The definitions of attack and recovery time in the CCITT recommendations are as follows:

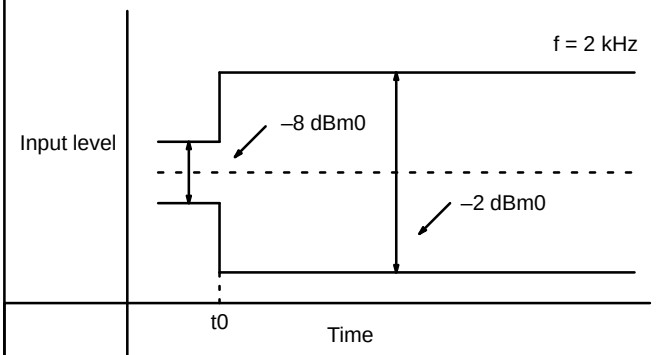
- Attack time = t1 (Output level reaches 150%) – t0 (Transient response starts)
- Recovery time = t1 (Output level reaches 75%) – t0 (Transient response starts)

2.2 Expander

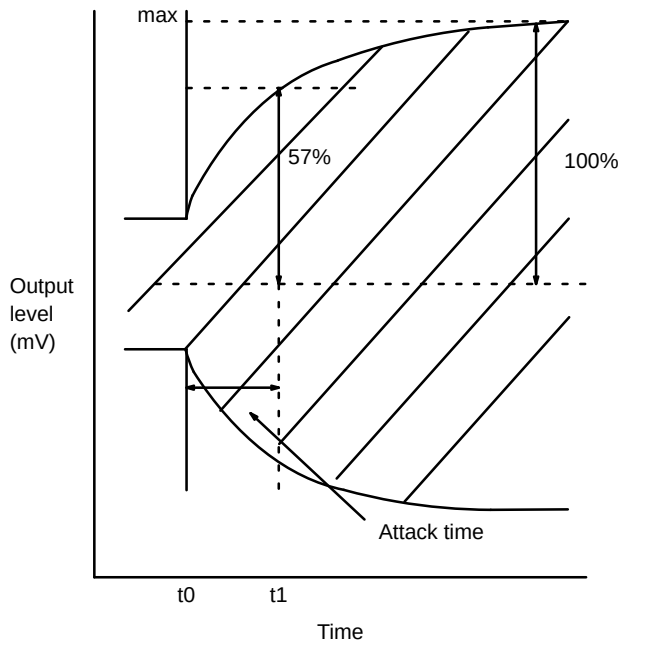
a. Attack time

- **Input conditions***

*When the reference input level to the expander is 0 dBm0, the input level is as follows:



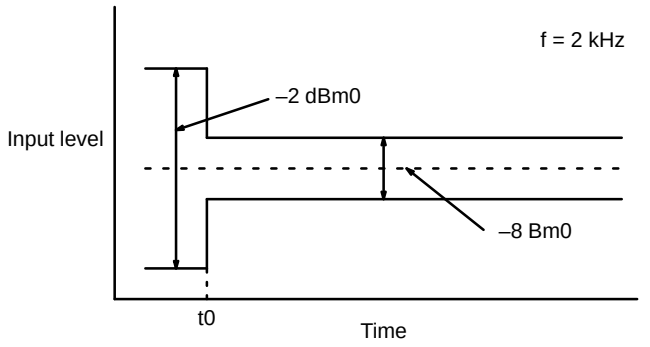
- **Output transient response characteristics**



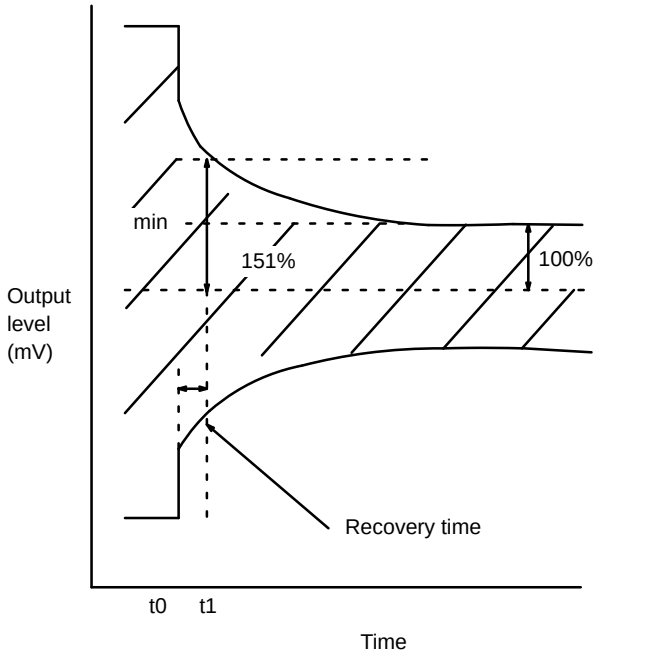
b. Recovery time

- **Input conditions***

*When the reference input level to the expander is 0 dBm0, the input level is as follows:



- **Output transient response characteristics**



Note: The definitions of attack and recovery time in the CCITT recommendations are as follows:

- Attack time = t1 (Output level reaches 57%) – t0 (Transient response starts)
- Recovery time = t1 (Output level reaches 151%) – t0 (Transient response starts)

ABSOLUTE MAXIMUM RATINGS

(A. GND and D. GND = 0 V, Ta = +25°C)

Parameter	Symbol	Pins	Values			Unit
			Min.	Typical	Max.	
Supply voltage	V_{DD}	V_{DDD}, V_{DDA}*	GND – 0.3	—	7	V
Input voltage	V_I	All input pins	GND – 0.3	—	V_{DD} + 0.3	V
Output voltage	V_O	All output pins	GND – 0.3	—	V_{DD} + 0.3	V
Output current	I_O	All output pins	–10	—	10	mA
Storage temperature	Tstg	—	–40	—	125	°C

*V_{DD} = VD_{DD} = VD_{DA}

RECOMMENDED OPERATING CONDITIONS

(A. GND and D. GND = 0 V)

Parameter	Symbol	Pins	Values			Unit
			Min.	Typical	Max.	
Power voltage	V_{DD}	V_{DDD}, V_{DDA}*	3.0**	5.0	5.5	V
Input voltage	V_{ID}	All digital input pin	0	—	V_{DD}	V
	V_{IA}	All analog input pin	1/4 V_{DD}	—	3/4 V_{DD}	V
Analog output voltage	V_{OA}	All analog input pin	1/4 V_{DD}	—	3/4 V_{DD}	V
Analog output load resistance***	RL_1	EMP_{OUT}, $TAMP_{OUT}$, MOD, $SAMP_{OUT}$, DEM_2, $RAMP_{OUT}$	10	—	—	kΩ
	RL_2	CMP_{OUT}, DSC_{OUT}, AF_{OUT}, CC_1, CC_3, CC_5, S_{OUT}	47	—	—	kΩ
	R_{L3}	AF_{IN2}	20	—	—	kΩ
Analog output load capacitance	C_L	All analog input pin	—	—	30	pF
OSC pin load capacitance	C_{OSC}	OSC_{IN}, OSC_{OUT}	20	30	50	pF
Operating ambient temperature	Ta	—	–30	25	70	°C
Transmission reference input level	T_{IN0}	AF_{IN1} – AF_{IN2}	—	$-20 + 20 \log_{10} (V_{DD}/3V)$	—	dBV
Reception reference input level	R_{IN0}	DEM_1 – DEM_2	—	$-14 + 20 \log_{10} (V_{DD}/3V)$	—	dBV

*V_{DD} = V_{DDD} = V_{DDA}

**Operation is possible up to 2.7 V, but the electrical characteristics are not guaranteed at 2.7 to 3.0 V.

***Resistance between all pins and 1/2 V_{DD} pin

DC CHARACTERISTICS

(V_{DD} = 3.0 to 5.5 V, A.GND and D.GND = 0 V, Ta = –30° to +70°C)

Parameter	Symbol	Pins	Conditions	Values			Unit
				Min.	Typical*	Max.	
Power supply current	$I_{DD}0$	V_{DDD}, V_{DDA}	Standby mode 0	4.5	8.5	19.0	mA
	$I_{DD}1$		Standby mode 1	4.0	8.4	18.5	mA
	$I_{DD}2$		Standby mode 2	2.5	5.2	12.5	mA
	$I_{DD}3$		Standby mode 3	1.2	2.5	7.5	mA
	$I_{DD}4$		Standby mode 4	0.1	0.5	2.0	mA
	$I_{DD}5$		Standby mode 5	—	50	250	µA
Low level input voltage	V_{IL}	All digital input pins	—	0	—	0.3 x V_{DD}	V
High level input voltage	V_{IH}		—	0.7 x V_{DD}	—	V_{DD}	V
Low level input current	I_{IL}	SD, SEND, D_{IN}, DCK, DSTB	V_I = 0 V	–10	—	10	µA
High level input current	I_{IH}		V_I = V_{DD}	–10	—	10	µA
Low level output voltage	V_{OL}	All digital output pins	I_{OL} = 0.5 mA	0	—	0.2 x V_{DD}	V
High level output voltage	V_{OH}		I_{OH} = –0.5 mA	0.8 x V_{DD}	—	V_{DD}	V
Pull-up resistance	R_{PLU}	RST, TEST	—	50	100	200	kΩ
Oscillation frequency	f_{OSC}	OSC_{IN}, OSC_{OUT}	—	—	3.6864	—	MHz
Analog input resistance 1	R_{AIN1}	1/2 V_{DDIN}	—	50	100	200	kΩ
Analog input resistance 2	R_{AIN3A}	LIM_{IN}	Between LIM_{IN} and 1/2V_{DD} during operation	10	20	40	kΩ
	R_{AIN3B}		Between LIM_{IN} and GND in PD	90	180	360	kΩ
Modulator output voltage	V_{MOT1}	S_{OUT}	During operation	0.16 x V_{DD}	0.2 x V_{DD}	0.24 x V_{DD}	V_{p-p}
	V_{MOT2}		Offset voltage during operation	1/2 V_{DD} – 0.3	1/2 V_{DD}	1/2 V_{DD} + 0.3	V
	V_{MOT3}		SEND = Low level	1/2 V_{DD} – 0.3	1/2 V_{DD}	1/2 V_{DD} + 0.3	V

*Typical value when V_{DD} = 3.0 V

(*Continued*)

(V_{DD} = 3.0 to 5.5 V, A.GND and D.GND = 0 V, Ta = –30° to +70°C)

Parameter	Symbol	Pins	Conditions	Values			Unit
				Min.	Typical*	Max.	
Limiter High level input voltage	V_{DLH}	$SAMP_{OUT}$	LIM_{IN} pin = open	1/2 V_{DD} + 0.04 V_{DD}	1/2 V_{DD} + 0.05 V_{DD}	1/2 V_{DD} + 0.06 V_{DD}	V
			LIM_{IN} pin = V_{LIM}**	1/2 V_{DD} + 0.8 x (1/2 V_{DD}–V_{LIM})	1/2 V_{DD} + 1.0 x (1/2 V_{DD} – V_{LIM})	1/2 V_{DD} + 1.2 x (1/2 V_{DD} – V_{LIM})	V
Limiter Low level input voltage	V_{DLL}	$SAMP_{OUT}$	LIM_{IN} pin = open	1/2 V_{DD} – 0.06 V_{DD}	1/2 V_{DD} – 0.05 V_{DD}	1/2 V_{DD} – 0.04 V_{DD}	V
			LIM_{IN} pin = V_{LIM}**	1/2 V_{DD} – 1.2 x (1/2 V_{DD} – V_{LIM})	1/2 V_{DD} – 1.0 x (1/2 V_{DD} – V_{LIM})	1/2 V_{DD} – 0.8 x (1/2 V_{DD} – V_{LIM})	V

*Typical value when V_{DD} = 3.0 V

**0 < V_{LIM} < 1/2 V_{DD} – 0.04 x V_{DD}

TRANSFER CHARACTERISTICS

1. Transmission

(V_{DD} = 3.0 to 5.5 V, A.GND and D.GND = 0 V, Ta = –30° to +70°C)

Parameter	Symbol	Pins	Conditions	Values			Unit
				Min.	Typical*	Max.	
Transmission gain	T_{GAIN1}	AF_{IN1} – MOD	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed	2.5	4.7	6.5	dB
Transmission gain 2	T_{GAIN2}	AF_{IN1} – EMP_{OUT}	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed	–1.5	–0.2	1.5	dB
Transmission gain 3	T_{GAIN3}	$SAMP_{OUT}$ – MOD	Input: 0 dB_{m0}, 1 kHz	7.5	8.3	9.5	dB
Mute level	T_{MUTE}	AF_{IN1} – MOD	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed, P message filter used, and in mute mode	—	–75	–60 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Signal-to-noise ratio	$T_{S/N}$	AF_{IN1} – MOD	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed, P message filter used	40	61	—	dB
Upper side band leak	T_{USB}	AF_{IN1} – MOD	Input: 0 dB_{m0}, 1 kHz When scrambler used and compandor bypassed	—	–81	–50	dB
Noise 1	T_{ICN1}	AF_{IN1} – MOD	No input When scrambler and P message filter used, and compandor bypassed	—	–68	–55 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Noise 2	T_{ICN2}	AF_{IN1} – MOD	No input When scrambler and compandor bypassed, and P message filter used	—	–75	–55 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Carrier leak	T_{CL}	AF_{IN1} – MOD	No input When scrambler used and the compandor bypassed, 3.338-kHz component	—	–86	–60	dBV
Original audio leak***	T_{LK}	AF_{IN1} – MOD	Input: 0 dB_{m0}, 1 kHz When scrambler used and the compandor bypassed — 3 V power	—	–56	–45	dB
			Input: 0 dB_{m0}, 1 kHz When scrambler used and the compandor bypassed — 5 V power	—	–41	–35	dB
BPF1 maximum input level	V_{IB1}	SCR_{IN}	Input: 0.3 to 3 kHz Compandor bypassed, input level in which distortion factor -34 dB, measured at CC1	–10 + 20 $\log_{10}$ (V_{DD}/3V)	–6	—	dBV

*Typical value when V_{DD} = 3.0 V

**Compounding ratio of 2.388 and 4.388 kHz

***Compounding ratio of 1 and 2.388 kHz

Notes:

1. See *Basic Circuits* for RC constant for external parts.
2. Reference input level: 0 dB_{m0} = -20 + 20 $\log_{10}$ (V_{DD}/3 V) dBV
3. Set to 0 dB for VOL1 and VOL2 (D8, D7, and D3 = “1”).
4. SEND = Low level
5. Select the after-frame-detection mode for demodulator output (D10 = “1”, D8 = “0”).
6. Set the carrier frequency to 3.388 kHz (D9 = “0”, D8 = “1”).

2. Reception

(V_{DD} = 3.0 to 5.5 V, A.GND and D.GND = 0 V, Ta = –30° to +70°C)

Parameter	Symbol	Pins	Conditions		Values			Unit
					Min.	Typical*	Max.	
Reception gain	R_{GAIN}	DEM_1 – $RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed		–1.5	–0.6	1.5	dB
Mute level	R_{MUTE}	DEM_1 – $RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed, P message filter used, and in mute mode		—	–87	–65 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Upper side band leak	R_{USB}	DEM_1 – $RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler used and compandor bypassed		—	–61	–50	dB
Signal-to-noise ratio	$R_{S/N}$	DEM_1 – $RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler and compandor bypassed, P message filter used, and in mute mode		40	60	—	dB
Noise 1	R_{ICN1}	DEM_1 – $RAMP_{OUT}$	No input When scrambler used compandor bypassed and P message filter used		—	–68	–55 + 20 $\log_{10}$ (V_{DD}/3 V)	dB
Noise 2	R_{ICN2}	DEM_1 – $RAMP_{OUT}$	No input When scrambler used compandor bypassed and P message filter used		—	–78	–55 + 20 $\log_{10}$ (V_{DD}/3 V)	dB
Carrier leak	R_{CL}	DEM_1 – $RAMP_{OUT}$	No input When scrambler used and compandor bypassed, 3.338-kHz component		—	–92	–65	dB
Original audio leak***	R_{LK}	DEM_1 – $RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler used and compandor bypassed	3 V power	—	–56	–45	dB
				5 V power	—	–41	–35	dB
BPF2 maximum input level	V_{IB2}	DEM_2	Input: 0.3 to 3 kHz Compandor bypassed, input level in which distortion factor -34 dB measured at CC3		–8 + 20 $\log_{10}$ (V_{DD}/3 V)	–5	—	dB

*Typical value when V_{DD} = 3.0 V

**Compounding ratio of 2.388 and 4.388 kHz

***Compounding ratio of 1 and 2.388 kHz

Notes:

1. See *Basic Circuits* for RC constant for external parts.
2. Reference input level: 0 dB_{mo} = –14 +20 $\log_{10}$ (V_{DD}/3 V) dBV
3. Set to 0 dB for VOL1 and VOL2 (D8, D7, and D3 = “1”).
4. SEND = Low level
5. Select the after-frame-detection mode for demodulator output (D10 = “1”, D8 = “0”).
6. Set the carrier frequency to 3.388 kHz (D9 = “0”, D8 = “1”).

3. Total Characteristics

(V_{DD} = 3.0 to 5.5 V, A.GND and D.GND = 0 V, Ta = –30° to +70°C)

Parameter	Symbol	Pins	Conditions		Values			Unit
					Min.	Typical*	Max.	
Signal-to-noise ratio 1	$A_{S/N1}$	AF_{IN1}–$RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler and P message filter used, compandor bypassed, and MOD pin connected to R4	3 V power	45	52	—	dB
				5 V power	40	47	—	dB
Signal-to-noise ratio 2	$A_{S/N2}$	AF_{IN1}–$RAMP_{OUT}$	Input: -30 dB_{m0}, 1 kHz When scrambler, P message filter, and compandor used, and MOD pin connected to R4		34	38	—	dB
Signal-to-noise ratio 3	$A_{S/N3}$	AF_{IN1}–$RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler, P message filter, and compandor used, and MOD pin connected to R4		36	50	—	dB
Signal-to-noise ratio 4	$A_{S/N4}$	AF_{IN1}–$RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When scrambler bypassed, compandor and P message filter used, and MOD pin connected to R4		40	55	—	dB
Transmission → reception crosstalk	XTC_1	AF_{IN1}–$RAMP_{OUT}$	AF_{IN1}: 0 dB_{m0}, 1 kHz DEM_1: No input When scrambler and compandor used		—	–82	–60	dB
Reception → transmission crosstalk	XTC_2	DEM_1–MOD	AF_{IN1}: No input DEM_1: 0 dB_{m0},1 kHz When scrambler and compandor used		—	–52	–30	dB
Total gain difference 1	D_{GAIN1}	AF_{IN1}–$RAMP_{OUT}$	Input: 0 dB_{m0}, 1 kHz When compandor used and MOD pin connected to R4 (Gain in use of scrambler) - (gain in bypass)		–3	–0.6	1	dB
Total gain difference 2	D_{GAIN2}	AF_{IN1}–$RAMP_{OUT}$	Input: 0 dB_{m0}, 400 Hz When compandor used and MOD pin connected to R4 (Gain in use of scrambler) - (gain in bypass)		–4.0	–2.5	0	dB
Total ICN	A_{ICN}	AF_{IN1}–$RAMP_{OUT}$	No input When scrambler, compandor, and P message filter used		—	–89	–79 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV

*Typical value when V_{DD} = 3.0 V

Notes:

1. See *Basic Circuits* for RC constant for external device.
2. Reference input level: 0dB_{m0} = -20 +20 $\log_{10}$ (V_{DD}/3 V) dBV
3. Set to 0 dB for VOL1 and VOL2 (D8, D7, and D3 = 1).
4. SEND = Low level
5. Select the after-frame-detection mode for demodulator output (D10 = 1, D8 = 0).
6. Set the carrier frequency to 3.388 kHz (D9 = 0, D8 = 1).

COMPANDOR CHARACTERISTICS

(V_{DD} = 3.0 to 5.5 V, A.GND = D.GND, Ta = –30°C to +70°C)

Parameter	Symbol	Pins	Conditions		Limits			Unit
					Min.	Typical*	Max.	
Compressor reference I/O level	V_{OC0}	AF_{IN1} – CMP_{OUT}	V_{IN} = –20.0 + 20 $\log_{10}$ (V_{DD}/3 V) dBV R1 = R2 Input: 1KHz		–21.5 + 20 $\log_{10}$ (V_{DD}/3 V)	–20.5 + 20 $\log_{10}$ (V_{DD}/3 V)	–18.5 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Compressor gain deviation	V_{OC1}	AF_{IN1} – CMP_{OUT}	R1 = R2 Input: 1 KHz	V_{IN} = +5 dB_{mo} to –40 dB_{mo}	–0.75	0.0	0.75	dB
	V_{OC2}			V_{IN} = –40 dB_{mo} to –45 dB_{mo}	–1.00	0.0	1.00	dB
	V_{OC3}			V_{IN} = –45 dB_{mo} to –50 dB_{mo}	–2.50	0.0	1.25	dB
Expander reference I/O level	V_{OE0}	EXP_{IN} – AF_{OUT}	Input: 1 KHz	V_{IN} = –14.0 + 20 $\log_{10}$ (V_{DD}/3 V) dBV	–16.0 + 20 $\log_{10}$ (V_{DD}/3 V)	–14.0 + 20 $\log_{10}$ (V_{DD}/3 V)	–12.0 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Expander gain deviation	V_{OE1}	EXP_{IN} – AF_{OUT}		V_{IN} = –2.5 dB_{mo} to –20 dB_{mo}	–1.0	0.0	1.0	dB
	V_{OE2}			V_{IN} = –20 dB_{mo} to –22.5 dB_{mo}	–1.25	0.0	1.25	dB
	V_{OE3}			V_{IN} = –22.5 dB_{mo} to –25 dB_{mo}	–2.50	0.0	1.25	dB
Compressor attack time	t_{ATC}	AF_{IN1} – CMP_{OUT}	CT1 = 0.1 µF R1 = R2	Input: –16 dB_{mo} → –4 dB_{mo}	2.0	4.0	5.0	ms
Compressor recovery time	t_{RCC}				7.0	14.0	20.0	ms
Expander attack time	t_{ATE}	EXP_{IN} – AF_{OUT}	CT2 = 0.1 µF	Input: –8 dB_{mo} → –2 dB_{mo}	2.0	4.0	5.0	ms
Compressor recovery time	t_{RCE}				7.0	14.0	20.0	ms
Compressor noise	C_{ICN}	AF_{IN1} – CMP_{OUT}	No input When P message filter used		—	—	–60 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV
Expander noise	E_{ICN}	EXP_{IN} – AF_{OUT}	No input When P message filter used		—	—	–79 + 20 $\log_{10}$ (V_{DD}/3 V)	dBV

*Typical value when V_{DD} = 3.0 V

Notes:

1. See *Basic Circuits* for RC constant for external device.
2. Set to 0 dB for VOL1 and VOL2 (D8, D7, and D3 = 1).

AC CHARACTERISTICS

(V_{DD} = 3.0 to 5.5 V, A.GND = D.GND, Ta = –30° to +70°C)

Parameter	Symbol	Pins	Conditions	Values			Unit
				Min.	Typical*	Max.	
SCK delay time 1	t_{dSC1}	SCK	—	208	265	417	µs
SCK delay time 2	t_{dSC2}	SCK	—	0	75	208	µs
FD_{OUT} delay time 1	t_{dFD1}	FD_{OUT}	—	0	—	1	µs
FD_{OUT} delay time 2	t_{dFD2}	FD_{OUT}	—	0	—	1	µs
SCK “L” level width	t_{wLS}	SCK	—	195	208	222	µs
SCK “H” level width	t_{wHS}	SCK	—	195	208	222	µs
SEND setup time	t_{suSE}	SEND	—	1	—	—	µs
SEND hold time	t_{hSE}	SEND	—	1	—	—	µs
SD setup time	t_{suSD}	SD	—	1	—	—	µs
SD hold time	t_{hSD}	SD	—	1	—	—	µs
S_{OUT} delay time 1	t_{dSO1}	S_{OUT}	—	0	—	20	µs
S_{OUT} delay time 2	t_{dSO2}	S_{OUT}	—	0	—	20	µs
S_{OUT} delay time 3	t_{dSO3}	S_{OUT}	—	0	—	10	µs
MSK input disable time	$t_{dR!}$	DEM_1, DEM_2	—	0	—	10	ms
Number of shift bits	N	—	No noise for DEM_1 and DEM_2	—	—	15	bit
Demodulator delay time	t_{dBD}	RD	$N \geq 15$ No noise for DEM_1 and DEM_2	761	975	1189	µs

*Typical value when V_{DD} = 3.0 V

Note: See *Basic Circuits* for RC constant for external parts.

(*Continued*) (V_{DD} = 3.0 to 5.5 V, A.GND = D.GND, Ta = –30° to +70°C)

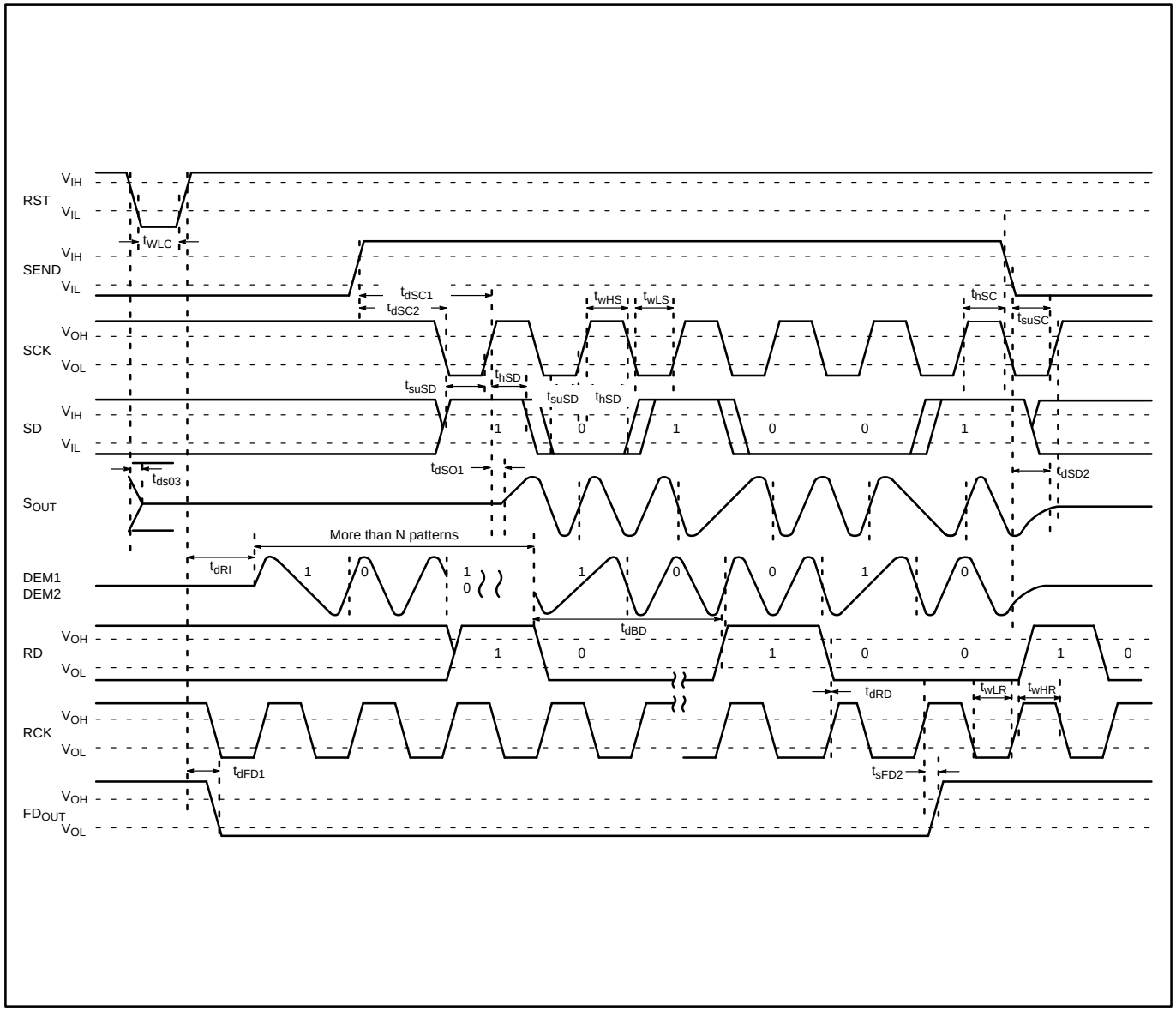
Parameter	Symbol	Pins	Conditions	Values			Unit
				Min.	Typical*	Max.	
RD timing	t_{dRD}	RD	—	–1	—	1	µs
RCK “L” level width	t_{wLR}	RCK	N ≥ 15 No noise for DEM_1 and DEM_2	169	208	248	µs
RCK “H” level width	t_{wHR}	RCK	N ≥ 15 No noise for DEM_1 and DEM_2	169	208	248	µs
RST “L” level width	t_{wLC}	RST	—	20	—	—	µs
Digital input rise time	t_r	RCK, SEND, SD, DCK, DSTB, D_{IN}	—	—	—	100	ns
Digital input fall time	t_f	RCK, SEND, SD, DCK, DSTB, D_{IN}	—	—	—	100	ns
D_{IN} setup time	t_{suD}	D_{IN}	—	100	—	—	ns
D_{IN} hold time	t_{hD}	D_{IN}	—	100	—	—	ns
Strobe setup time	t_{suT}	DSTB	—	100	—	—	ns
DCK “L” level width	t_{wLD}	DCK	—	100	—	—	ns
DCK period	t_{wWD}	DCK	—	2	—	—	µs
Strobe “L” level width	t_{wLT}	DSTB	—	100	—	—	ns

*Typical value when V_{DD} = 3.0 V

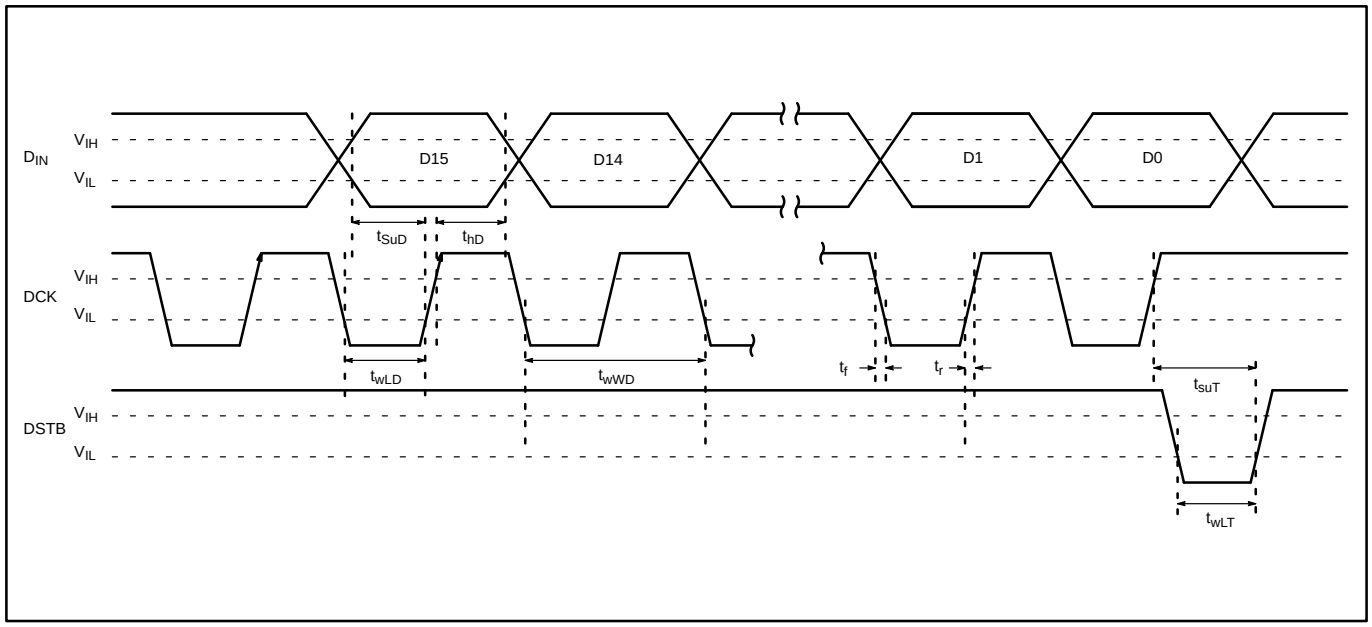
Note: See *Basic Circuits* for RC constant for external device.

TIMING CHARTS

1. MSK Modem Timing

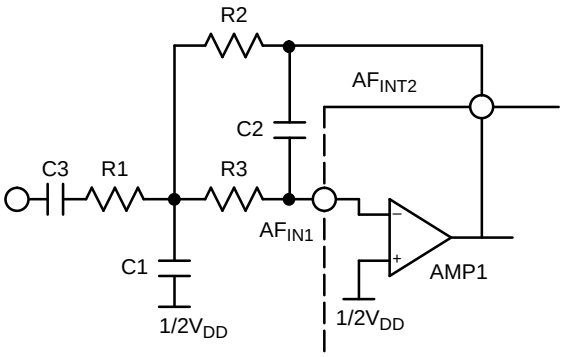


2. Serial Interface Timing



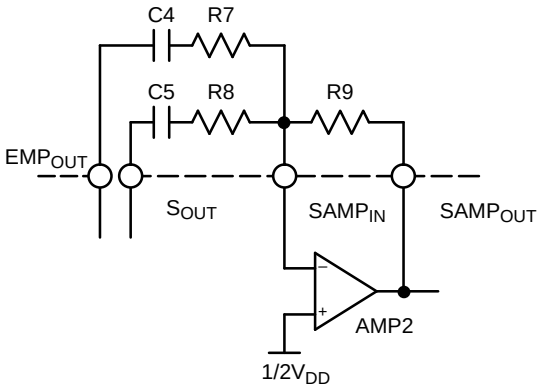
BASIC CIRCUITS

1. AMP1



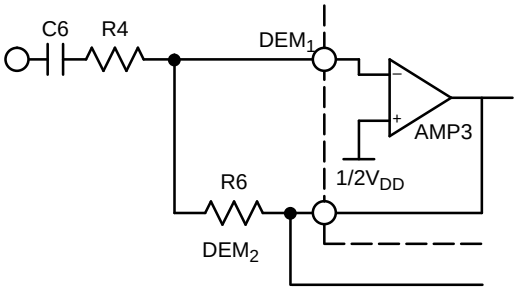
R1 = 22 kΩ
R2 = 22 kΩ
R3 = 22 kΩ
C1 = 3300 pF
C2 = 820 pF
C3 = 0.1 µF

2. AMP2



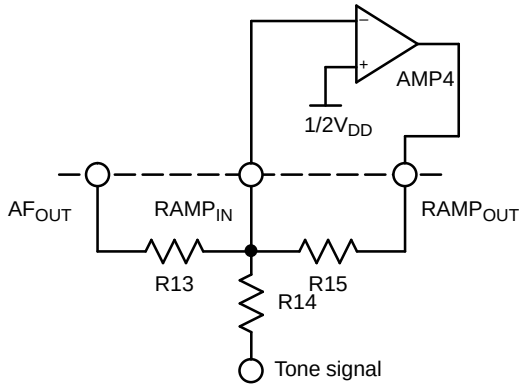
R7 = 68 kΩ
R8 = 150 kΩ
R9 = 47 kΩ
C4 = 0.1 µF
C5 = 0.1 µF

3. AMP3



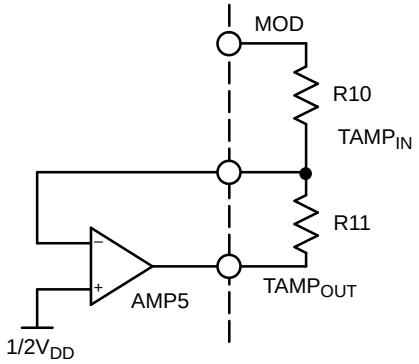
R4 = 47 kΩ
R6 = 47 kΩ
C6 = 0.1 µF

4. AMP4



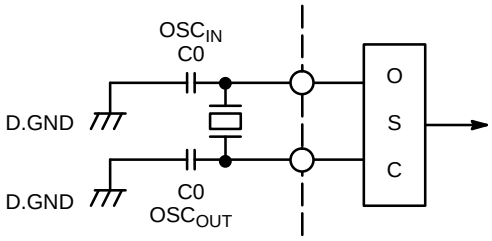
R13 = 47 kΩ
R14 = 47 kΩ
R15 = 47 kΩ

5. AMP5



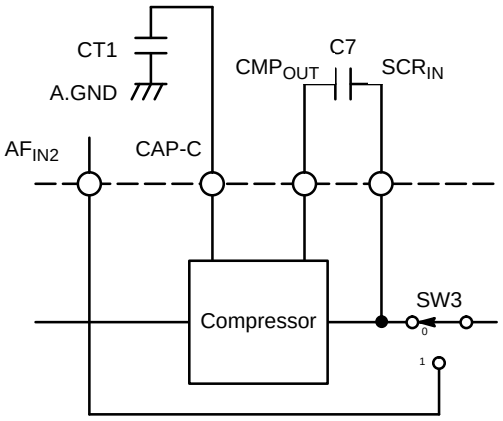
R10 = 47 kΩ
R11 = 47 kΩ

6. Crystal oscillator circuit



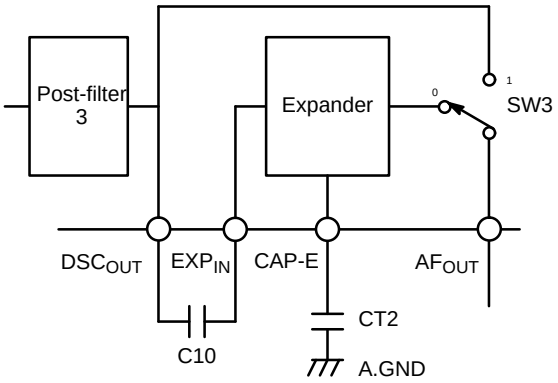
C0 = 22 pF

7. Compressor



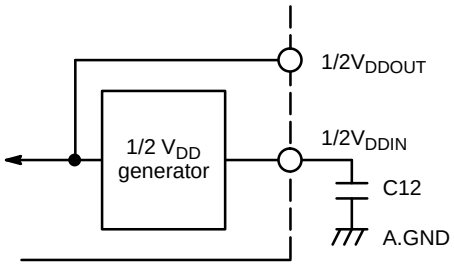
CT1 = 0.1 µF
C7 = 0.047 µF

8. Expander



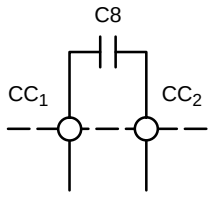
CT2 = 0.1µF
C10 = 0.047 µF

9. 1/2 V_{DD} Generator

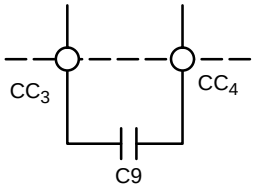


C12 = 1 µF

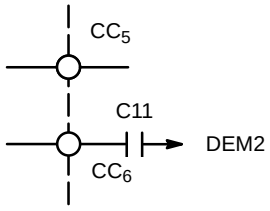
10. DC-cut Capacitor



C8 = 0.047 µF

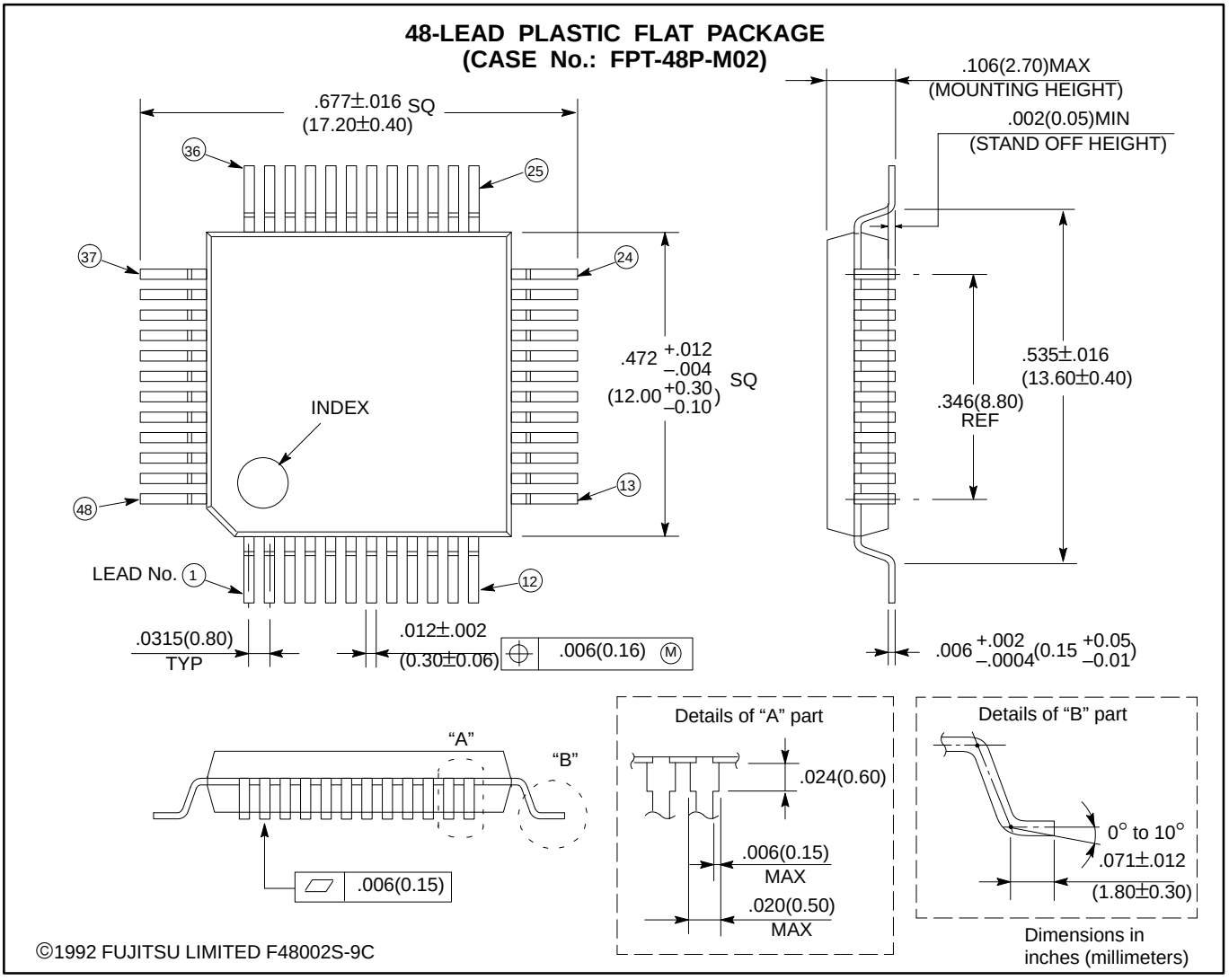


C9 = 0.047 µF



C11 = 0.047 µF

PACKAGE DIMENSIONS



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