FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–22204–2E

ASSP

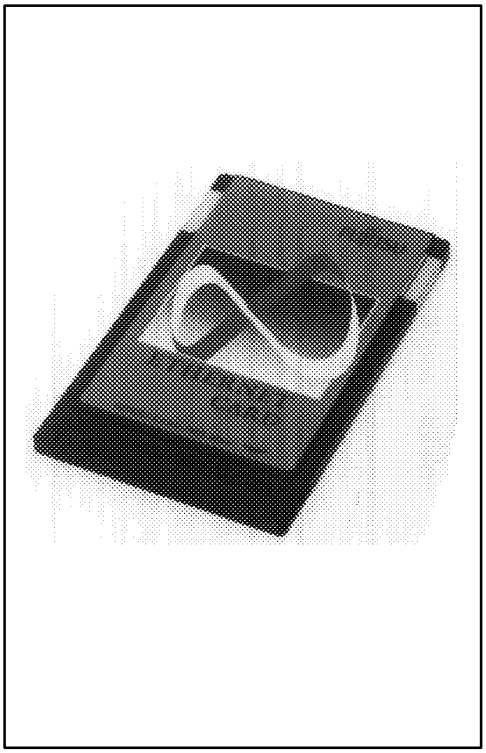
LAN CARD

MBH10302

Compatible with PCMCIA*1 and JEIDA*2

The Ethernet-type personal-computer Local Area Network (LAN) is gaining rapid and widespread acceptance, continuing the trend toward downsized hardware and networked computer equipment. The MBH10302 LAN card is compatible with the 10Base-T standard for 10-Mbps transmission over up to 100 m of twisted-pair cable, which is suitable for an office LAN requiring network expansion.

The MBH10302 incorporates an interface circuit compatible with PCMCIA and JEIDA. Therefore, it can be easily used by installing it in small OA equipment, such as PCs, handy terminals, and POSs, with the JEIDA I/O card interface and by connecting the 9-pin connector to a hub (line concentrator) with a special cable.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Features

- JEIDA IC Memory Card Guideline Ver. 4.1
- PCMCIA Release 2.0
- Ethernet 10Base-T standard and IEEE 802.3
- FCC class A
- Data transmission speed: 15 Mbps in 16-bit mode, 7 Mbps in 8-bit mode
- Internal E^2PROM and SRAM (32 K × 8)
- Common mode filter including crystal oscillator and transformer
- JEIDA type-II architecture
- Loopback auto-diagnostic function
- Non-intelligent type card
- Netware*3, LAN Manager*4 and TCP-IP drivers supported

Notes:
1. PCMCIA: Personal Computer Memory Card International Association
2. JEIDA: Japan Electronic Industry Development Association
3. Netware is a trademark of Novel, Inc.
4. LAN Manager is a trademark of Microsoft Corporation.

PRELIMINARY

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PIN ASSIGNMENT

1. I/O Interface (68-pin connector)

This Ethernet card supports the JEIDA 4.1 and PCMCIA 2.0 I/O interfaces.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	18	NC	35	GND	52	NC
2	D3	19	NC	36	$\overline{CD1}$	53	NC
3	D4	20	NC	37	D11	54	NC
4	D5	21	NC	38	D12	55	NC
5	D6	22	A7	39	D13	56	NC
6	D7	23	A6	40	D14	57	NC
7	$\overline{CE1}$	24	A5	41	D15	58	RESET
8	A10	25	A4	42	$\overline{CE2}$	59	$\overline{WAIT}$
9	$\overline{OE}$	26	A3	43	NC	60	$\overline{INPACK}$
10	A11	27	A2	44	$\overline{IORD}$	61	$\overline{REG}$
11	A9	28	A1	45	$\overline{IOWR}$	62	($\overline{SPKR}$)
12	A8	29	A0	46	NC	63	$\overline{STSCHG}$
13	NC	30	D0	47	NC	64	D8
14	NC	31	D1	48	NC	65	D9
15	$\overline{WE}$	32	D2	49	NC	66	D10
16	$\overline{IREQ}$	33	$\overline{IOIS16}$	50	NC	67	$\overline{CD2}$
17	V_{CC}	34	GND	51	V_{CC}	68	GND

2. Driver Interface (9-pin connector)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TD+	4	NC	7	NC
2	NC	5	NC	8	RD+
3	TD–	6	NC	9	RD–

*NC: No connection

PIN DESCRIPTION

1. I/O Interface (68-pin connector)

Pin No.	Pin name	I/O	Descriptions	Internal pin processing
2 to 6, 30 to 32, 37 to 41, 64 to 66	D0 to D15	I/O	**Data bus**: The MSB is D15 and the LSB is D0.	PULL-DOWN 220 kΩ
8, 10 to 12, 22 to 29	A0 to A11	I	**Address bus**: The MSB is A11 and the LSB is A0. A0 is invalid in word access.	PULL-DOWN 220 kΩ
7	$\overline{CE1}$	I	**Card enable (CE1 and CE2)**: Used to access attribute memory $\overline{CE1}$ enables even-address bytes and $\overline{CE2}$ enables odd-address bytes. These pins must be High level for 20 ms after applying V_{CC} to the card or releasing reset.	PULL-UP 50 kΩ
42	$\overline{CE2}$			
9	$\overline{OE}$	I	**Output enable**: Used to control-read data from card This pin must be inactive during write operations.	PULL-UP 100 kΩ
15	$\overline{WE}$	I	**Write enable**: Used to control write-operation data to card	PULL-UP 100 kΩ
36	$\overline{CD1}$	O	**Card detect (CD1 and CD2)**: Generates card detection signal Since these pins are grounded internally on the card, the system interface can detect card insertion /pull-out by providing a 10 kΩ or larger pull-up resistor at VCC.	GND
67	$\overline{CD2}$			
61	$\overline{REG}$	I	**Attribute memory space select**: Must be kept High level (inactive) for memory access When this pin is Low level (active), access is limited to the attribute memory by activating the $\overline{OE}$ or $\overline{WE}$ pins, and to the I/O space by activating the $\overline{IORD}$ or $\overline{IOWR}$ pins. Since the attribute memory is allocated at even addresses, only data signals D0 to D7 are valid; D8 to D15 are ignored for word access. Odd addresses are invalid for byte access. I/O space is used for accessing peripheral devices. Systems that set the $\overline{IORD}$ and $\overline{IOWR}$ pins to Low level during DMA operations must have the $\overline{REG}$ pin kept High level (inactive) during DMA transfers to prevent erroneous I/O access.	PULL-UP 100 kΩ
58	RESET	I	**Reset**: Clears CCR register to place card in unconfigured state (IC card interface) This also starts initializing the additional card. The system must keep this pin at high impedance for 1 ms after stabilization of the power supply during card power-up.	PULL-UP 100 kΩ

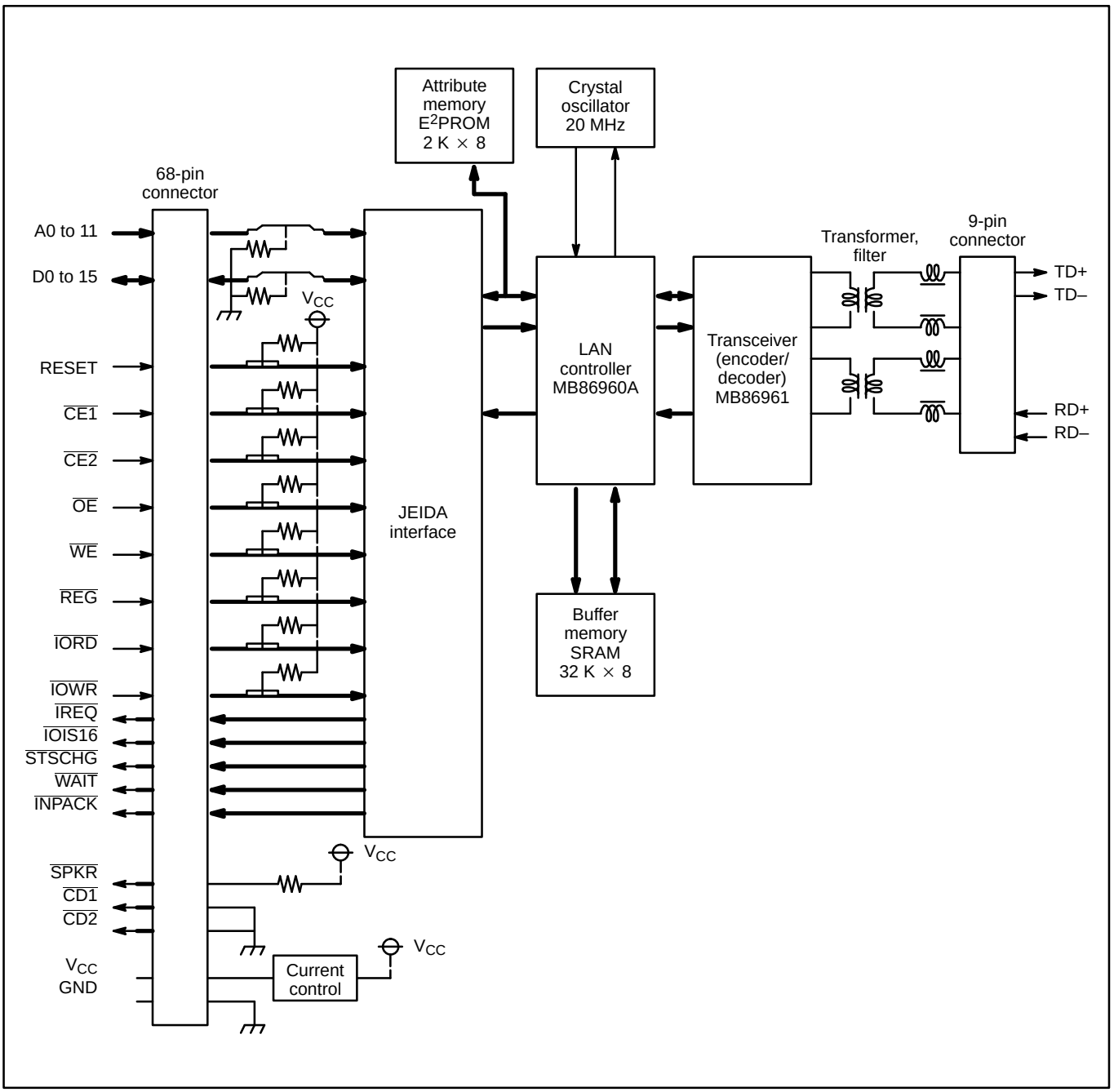
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Pin No.	Pin name	I/O	Descriptions	Internal pin processing
59	$\overline{\text{WAIT}}$	O	**Wait**: Delays completion of I/O access cycle in progress The card outputs Low level to this pin.	C-MOS Output
44	$\overline{\text{IORD}}$	I	**I/O Read**: Reads data from card I/O space The card will not respond to this pin until the I/O card interface mode is set.	PULL-UP 100 kΩ
45	$\overline{\text{IOWR}}$	I	**I/O Write**: Writes data to card I/O space The card will not respond to this pin until the I/O card interface mode is set.	PULL-UP 100 kΩ
60	$\overline{\text{INPACK}}$	O	**Input Acknowledge:** The card outputs Low level to this pin (active) when the $\overline{\text{CE}}$ and $\overline{\text{IORD}}$ pins are Low level and the address on the address bus corresponds to the I/O ports of the card. This pin is used to control enable of the input data buffer for the system interface.	C-MOS Output
33	$\overline{\text{IOIS16}}$	O	**16-bit I/O port**: The card outputs Low level to this pin (active) when the I/O port being addressed at the interface is capable of 16-bit access. When this pin is High level (inactive) during 16-bit access, the system will perform 8-bit access to the even and odd bytes of the objected 16-bit port.	C-MOS Output
16	$\overline{\text{IREQ}}$	O	**Interrupt request**: Available only in I/O operation mode The I/O card outputs Low level (active) to this pin to ask the system for software service. When no interrupt is requested, a High level is output (inactive). An interrupt signal is transmitted to one of the interrupt request pins on the system internal bus via the socket interface.	C-MOS Output
62	$\overline{\text{(SPKR)}}$	O	**Digital voice output**: Since the MBH10302 does not support this function, this pin is held at High level (inactive).	PULL-UP 4.7 kΩ
63	$\overline{\text{STSCHG}}$	O	**Status changed**: Alerts system to changes in ready or busy conditions of card while I/O card interface mode is set.	C-MOS Output
17, 51	$\overline{V_{CC}}$	—	**Power supply**: +5 V ±5%	
1, 34, 35, 68	$\overline{\text{GND}}$	—	**Ground**	
18, 19, 43 13 to 14 20 to 21 46 to 50 52 to 57	$\overline{\text{NC}}$	—	No connection	

2. Transceiver Interface (9-pin connector)

Pin No.	Pin name	I/O	Descriptions
1, 3	TD+ TD–	O	Differential output pin for twisted-pair transmission data. It is connected to the internal transformer.
8, 9	RD+ RD–	I	Differential input pin for twisted-pair reception data. It is connected to the internal transformer.
2, 4 to 7	NC	—	No connection

BLOCK DIAGRAM



MEMORY

1. Memory Map

The system switches to the IC memory card interface when the MBH10302 is inserted.

The memory address spaces of the IC memory card are as follows:

(1) Common memory: Stores user data

(2) Attribute memory: Stores card attributes in card information structure (CIS) and configuration data in CCR register

The system reads from and writes to the attribute memory when the card is inserted.

Writing to the CCR register switches the system to the I/O interface mode and starts the I/O card function.

2. Memory Address Space

2.1 Attribute memory space

Attribute memory access is valid only for even bytes.

The attribute memory is the following two areas selected by the $\overline{REG}$, $\overline{WE}$, and $\overline{OE}$ signals.

(1) Card information structure (CIS): Stores card capabilities and specifications

(2) Card configuration register (CCR): The card operation environment is specified by the system.

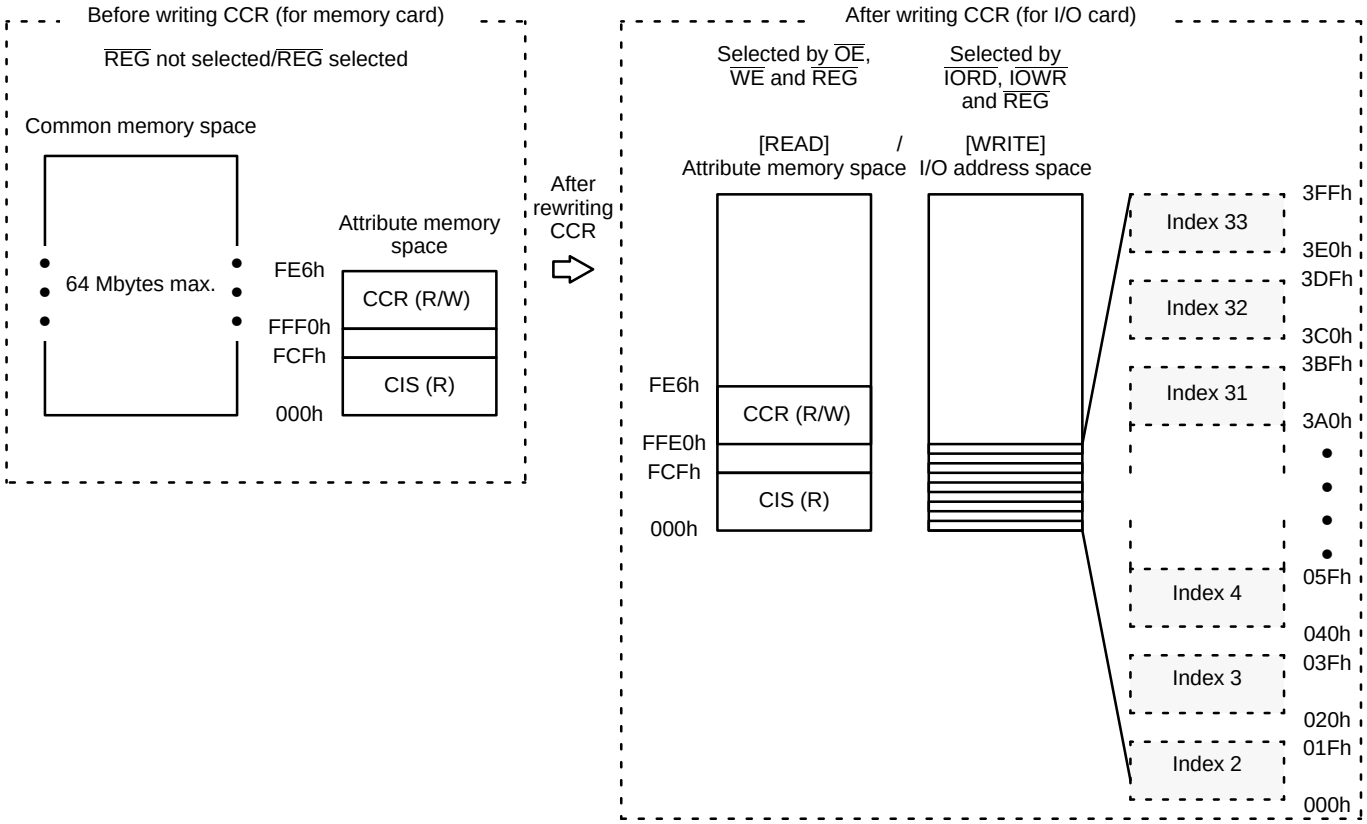
The CIS starts from address 0 but need not be contiguous region.

See *Attribute Memory Register* for the attribute data.

2.2 I/O mode memory space

The I/O mode memory space is an I/O card interface space selected by the $\overline{REG}$, $\overline{TORD}$, and $\overline{TOWR}$ signals.

Access to the attribute memory is also available in the I/O mode. (In this mode, the system refers to the CCR contents.)



3. Switching to I/O Card from Memory Card

The I/O card switches to the I/O card interface mode when it is programmed by the system to use the I/O card interface using the internal CCR. Before this programming, the system must check the CIS to determine the I/O address space, interrupt request, and other program environments. The system specifies the optimum operation environment by comparing the contents of the CIS and requests from other cards in the system to maintain compatibility between the system hardware and software.

Writing to the configuration index at address FE0h of the CCR by the system automatically switches the card to the I/O mode.

Requirements for writing to CCR by system OS

V_{CC} = 5 V

The CCR must not be rewritten after changing to the I/O card mode. (If necessary, reset the system.)

4. Initializing to I/O Mode

- Use the configuration index signal of the attribute memory as a trigger signal.
- Do not return the system OS to the IC memory mode after initializing to the I/O mode.
- The system must not access the card until initialization of the I/O mode register is completed (during I/O card initialization). Wait for 20 ms.

5. Memory Space Select

5.1 Common memory access (for memory card)

$\overline{CE1}$	$\overline{REG}$	$\overline{WE}$	$\overline{OE}$	A0	VPP1 VPP2	A1 to A11	I/O pins (D0 to D15)
H	×	×	×	×	V_{CC}	×	High-Z
H	H	×	×	×	V_{CC}	×	High-Z
L	H	×	×	L	V_{CC}	×	Even address
L	H	×	×	H	V_{CC}	×	Odd address
L	H	×	×	×	V_{CC}	×	Even byte

Note: Write when the $\overline{OE}$ pin is High and the $\overline{WE}$ pin is Low; read by vice *versa*.

5.2 Attribute memory access (for memory card and I/O card)

$\overline{CE1}$	$\overline{REG}$	$\overline{WE}$	$\overline{OE}$	A0	VPP1 VPP2	A1 to A11	Operation mode	I/O pins (D0 to D15)
H	×	×	×	×	V_{CC}	×		High-Z
H	L	H	L	×	V_{CC}	×		High-Z
L	L	H	L	L	V_{CC}	×	READ	Even byte
L	L	H	L	H	V_{CC}	×	READ	Invalid
L	L	H	L	×	V_{CC}	×	READ	Even byte
H	L	L	H	×	V_{CC}	×		don't care
L	L	L	H	L	V_{CC}	×	WRITE	Even byte
L	L	L	H	H	V_{CC}	×	WRITE	don't care
L	L	L	H	×	V_{CC}	×	WRITE	don't care

Note: The $\overline{CE2}$ pin is not used because even addresses are used in accessing the attribute memory.

REGISTER DATA

1. Attribute Memory Registers

1.1 Card information structure (CIS)

Byte	Tuple ID	Tuple name	Description
000h	01h	CISTPL DEVICE	Device information tuple (for common memory)
002h	03h	TPL LINK	Pointer for next tuple
004h	DCh	Device information	

7	6	5	4	3	2	1	0
Device types D: I/O device				WPS 1: Invalid	Device speed 4: 100 ns		

006h	03h	Device size	

7	6	5	4	3	2	1	0
Mantissa 00h:					Exponent 3h: 32 Kbyte		

008h	FFh		End of device information
00Ah	17h	CISTPL DVICE A	Device information tuple (for attribute memory)
00Ch	05h	TPL LINK	Pointer for next tuple
00Eh	4Bh	Device information 1	

7	6	5	4	3	2	1	0
Device types 4h: E^2PROM				WPS 1: Invalid	Device size 3h: 150 ns		

010h	01h	Device size	

7	6	5	4	3	2	1	0
Mantissa 00h:					Exponent 1h: 2 Kbyte		

012h	DCh	Device information 2	

7	6	5	4	3	2	1	0
Device types Dh: I/O device				WPS 1: Invalid	Device size 4h: 100 ns		

014h	00h	Device size	

7	6	5	4	3	2	1	0
Mantissa 00h:					Exponent 0h: 512 byte		

Byte	Tuple ID	Tuple name	Description
016h	FFh		End of device information
018h	20h	CISTPL MANFID	
01Ah	05h	TPL LINK	Pointer for next tuple
01Ch	04h	TPLMID MANF	JEDEC manifacture ID: Fujitsu JEDEC ID 0 × 0004
01Eh	00h		MSB
020h	04h		Card version No.: 0 × 0004
022h	00h		MSB
024h	FFh		End of JEDEC information
026h	21h	CISTPL FUNCID	
028h	03h	TPL LINK	Pointer for next tuple
02Ah	06h	TPLFID FUNCTION	JEDEC device ID: Network Adapter
02Ch	00h		
02Eh	FFh		End of JEDEC information
030h	15h	CISTPL VERS 1	Level 1 version/product information tuple
032h	2Ah	TPL LINK	Pointer for next tuple
034h	04h	TPLLV1 MAJOR	Upper specification version
036h	01h	TPLLV1 MINOR	Lower specification version
038h	46h	TPLLV1 INFO	Manufacture information (F)
03Ah	55h		(U)
03Ch	4Ah		(J)
03Eh	49h		(I)
040h	54h		(T)
042h	53h		(S)
044h	55h		(U)
046h	00h		End ID of manufactureinformation
048h	45h		Product version information 1 (E)
04Ah	54h		(T)
04Ch	48h		(H)
04Eh	45h		(E)
050h	52h		(R)
052h	4Eh		(N)
054h	45h		(E)
056h	54h		(T)
058h	20h		( )
05Ah	4Ch		(L)
05Ch	41h		(A)
05Eh	4Eh		(N)
060h	20h		( )

Byte	Tuple ID	Tuple name	Description
062h 064h 066h 068h 06Ah 06Ch 06Eh 070h 072h 074h 076h 078h 07Ah	4Dh 42h 48h 31h 30h 33h 30h 32h 20h 20h 30h 34h 00h		(M) (B) (H) (1) (0) (3) (0) (2) ( ) ( ) (0) (1) End ID of product version information 1
07Ch 07Eh 080h 082h 084h	20h 20h 30h 35h 00h		Product version information 2 ( ) ( ) (0) (1) End ID of product version information 2
086h	FFh		End of level 1 version /product information
088h	14h	CISTPL NO LINK	No link tuple
08Ah	01h	TPL LINK	Pointer for next tuple
08Ch	FFh		
08Eh	1Ah	CISTPL CONF	Configuration tuple
090h	07h	TPL LINK	Pointer for next tuple
092h	05h	TPCC SZ	Field size byte
094h	21h	TPCC LAST	Configuration table last entry index Index = 33
096h 098h	E0h 0Fh	TPCC RADR	Configuration register base address “FFE0h”
09Ah 09Ch	0Fh 00h	TPCC RMSK	Configuration register presence mask “000Fh”
09Eh	FFh		
0A0h	1Bh	CISTPL CE	Configuration entry tuple
0A2h	18h	TPL LINK	Pointer for next tuple
0A4h	C1h	TPCE INDX	Configuration index byte

7	6	5	4	3	2	1	0
TPCC RFSZ (TPCC RSVD Field size 0: 0 byte		TPCC RMSZ TPPC RMSK field size 1: 2 byte				TPCC RASZ TPCC RADR field size 1: 2 bytes	

7	6	5	4	3	2	1	0
Intface 1:	Default 1:	Configuration index 01h: Index = 1					

Byte	Tuple ID	Tuple name	Description
0A6h	C1h	TPCE IF	Interface description field

7	6	5	4	3	2	1	0
M Wait Required 1:	ReadyBusy Active 1:	WP Active 0:	BVD Active 0:	Interface type 1: I/O card interface			

0A8h	FDh	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 1:	Memory space 3:		IRQ 1:	IO space 1:	Timing 0:	Power 1: V_{CC}	

0AAh	5Fh	TPCE PD	Power description structure parameter selection

Byte	7	6	5	4	3	2	1	0
0	RFU (0) 0:	PDwn I 1:	Peak I 0:	Avg I 1:	Static I 1:	Max V 1:	Min V 1:	Nom V 1:

0ACh	55h	Parameter definition (Nom V = +5 V)

Byte	7	6	5	4	3	2	1	0
0	EXT 0:	Mantissa Ah: 5				Exponent 5: 1 V		

0AEh 0B0h	C5h 4Bh	Parameter definition (Min V = 4.75 V)

Byte	7	6	5	4	3	2	1	0
0	EXT 1:	Mantissa 8h: 4				Exponent 5: 1 V		
1	0:	Extension: 75						

0B2h 0B4h	D5h 19h	Parameter definition (Max V = +5.25 V)

Byte	7	6	5	4	3	2	1	0
0	EXT 1:	Mantissa Ah: 5				Exponent 5: 1 V		
1	0:	Extension: 25						

0B6h 0B8h	86h 10h	Parameter definition (Static I = 116 mA)

Byte	7	6	5	4	3	2	1	0
0	EXT 1:	Mantissa 0h: 1				Exponent 6: 100 mA		
1	0:	Extension: 16						

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>0BAh</td><td>26h</td><td colspan="2">Parameter definition (Avg I = 200 mA)
<table>
<tr><td>Byte</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>EXT
1:</td><td colspan="4">Mantissa
4h: 2</td><td colspan="3">Exponent
6: 100 mA</td></tr>
</table></td></tr>
<tr><td>0BCh</td><td>45h</td><td colspan="2">Parameter definition (PDwn I = 40 mA)
<table>
<tr><td>Byte</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>EXT
0:</td><td colspan="4">Mantissa
4h: 4</td><td colspan="3">Exponent
5: 10 mA</td></tr>
</table></td></tr>
<tr><td>0BEh</td><td>E0h</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>Byte</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0:</td></tr>
</table></td></tr>
<tr><td>0C0h</td><td>40h</td><td colspan="2">I/O range description byte
<table>
<tr><td>Byte</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
0:</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>0C2h</td><td>1Fh</td><td></td><td>Length field (length of I/O address block – 1)</td></tr>
<tr><td>0C4h</td><td>30h</td><td>TPCE IR</td><td>Interrupt request information
<table>
<tr><td>Byte</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">Share
0:</td><td rowspan="2">Pulse
1:</td><td rowspan="2">Level
0:</td><td rowspan="2">Mask
0:</td><td colspan="4">IRQN 0h:</td></tr>
<tr><td>VEND</td><td>BERR</td><td>IOCK</td><td>NMI</td></tr>
<tr><td>1</td><td>IRQ7</td><td>IRQ6</td><td>IRQ5</td><td>IRQ4</td><td>IRQ3</td><td>IRQ2</td><td>IRQ1</td><td>IRQ0</td></tr>
<tr><td>2</td><td>IRQ15</td><td>IRQ14</td><td>IRQ13</td><td>IRQ12</td><td>IRQ11</td><td>IRQ10</td><td>IRQ9</td><td>IRQ8</td></tr>
</table></td></tr>
<tr><td>0C6h</td><td>FFh</td><td colspan="2"></td></tr>
<tr><td>0C8h</td><td>FFh</td><td colspan="2"></td></tr>
<tr><td>0CAh</td><td>28h</td><td>TPCE MS</td><td>Memory space information
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Host address
0:</td><td colspan="2">Card base address
1: 1 byte</td><td colspan="2">Window size
1: 1 byte</td><td colspan="3">Number of windows
0:</td></tr>
</table></td></tr>
<tr><td>0CCh</td><td>80h</td><td></td><td>Window page size (128 × 256 byte)</td></tr>
<tr><td>0CEh</td><td>00h</td><td></td><td>Card base address (00h)</td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>0D0h</td><td>20h</td><td>TPCE MI</td><td>Miscellaneous Function Information
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Extension
0:</td><td>Reserved
(0)
0:</td><td>Power-
down
1:</td><td>Read only
0:</td><td>Audio
0:</td><td colspan="3">Max. twin card
0:</td></tr>
</table></td></tr>
<tr><td>0D2h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>0D4h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>0D6h</td><td>07h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>0D8h</td><td>02h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
02h: Index 2</td></tr>
</table></td></tr>
<tr><td>0DAh</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>0DCh</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>0DEh</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>0E0h</td><td>00h</td><td></td><td>Address field (start of I/O address block) “00h”</td></tr>
<tr><td>0E2h</td><td>1Fh</td><td></td><td>Length field (size: 32 byte)</td></tr>
<tr><td>0E4h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>0E6h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>0E8h</td><td>07h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>0EAh</td><td>03h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
03h: Index 3</td></tr>
</table></td></tr>
</table>

Byte	Tuple ID	Tuple name	Description
0ECh	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

0EEh	EAh	TPCE IO	I/O space information

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

0F0h	60h		

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

0F2h	20h		Address field (start of I/O address block) “20h”
0F4h	1Fh		Length field (size: 32 byte)
0F6h	FFh		
0F8h	1Bh	CISTPL CE	Configuration entry tuple
0FAh	07h	TPL LINK	Pointer for next tuple
0FCh	04h	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 04h: Index 4					

0FEh	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

100h	EAh	TPCE IO	I/O space information

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

102h	60h		

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

Byte	Tuple ID	Tuple name	Description
104h	40h		Address field (start of I/O address block) “40h”
106h	1Fh		Length field (Size: 32 byte)
108h	FFh		
10Ah	1Bh	CISTPL CE	Configuration entry tuple
10Ch	07h	TPL LINK	Pointer for next tuple
10Eh	05h	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 05h: Index 5					

110h	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella- neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

112h	EAh	TPCE IO	I/O space information

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

114h	60h

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

116h	60h		Address field (start of I/O address block) “60h”
118h	1Fh		Length field (Size: 32 byte)
11Ah	FFh		
11Ch	1Bh	CISTPL CE	Configuration entry tuple
11Eh	07h	TPL LINK	Pointer for next tuple
120h	06h	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 06h: Index 6					

122h	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella- neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>124h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>126h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>128h</td><td>80h</td><td></td><td>Address field (start of I/O address block) “80h”</td></tr>
<tr><td>12Ah</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>12Ch</td><td>FFh</td><td></td><td></td></tr>
<tr><td>12Eh</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>130h</td><td>07h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>132h</td><td>07h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
07h: Index 7</td></tr>
</table></td></tr>
<tr><td>134h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>136h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>138h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
1: 1 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>13Ah</td><td>A0h</td><td></td><td>Address field (start of I/O address block) “A0h”</td></tr>
<tr><td>13Ch</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>13Eh</td><td>FFh</td><td></td><td></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>140h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>142h</td><td>07h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>144h</td><td>08h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
08h: Index 8</td></tr>
</table></td></tr>
<tr><td>146h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>148h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>14Ah</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>14Ch</td><td>C0h</td><td></td><td>Address field (start of I/O address block) “C0h”</td></tr>
<tr><td>14Eh</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>150h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>152h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>154h</td><td>07h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>156h</td><td>09h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
09h: Index 9</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>158h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>15Ah</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>15Ch</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>15Eh</td><td>E0h</td><td></td><td>Address field (start of I/O address block) “E0h”</td></tr>
<tr><td>160h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>162h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>164h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>166h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>168h</td><td>0Ah</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
0Ah: Index 10</td></tr>
</table></td></tr>
<tr><td>16Ah</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
</table>

Byte	Tuple ID	Tuple name	Description
16Ch	EAh	TPCE IO	I/O space information
16Eh	60h		I/O space description byte I/O range description byte
170h	00h		Address field (start of I/O address block) “0100h”
172h	01h		
174h	1Fh		Length field (Size: 32 byte)
176h	FFh		
178h	1Bh	CISTPL CE	Configuration entry tuple
17Ah	08h	TPL LINK	Pointer for next tuple
17Eh	0Bh	TPCE INDX	Configuration table index byte
180h	08h	TPCE FS	Function selection byte
182h	EAh	TPCE IO	I/O space information
184h	60h		I/O space description byte I/O range description byte

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 0Bh: Index 11					

Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

Byte	Tuple ID	Tuple name	Description
186h	20h		Address field (start of I/O address block) “0120h”
188h	01h		
18Ah	1Fh		Length field (Size: 32 byte)
18Ch	FFh		
18Eh	1Bh	CISTPL CE	Configuration entry tuple
190h	08h	TPL LINK	Pointer for next tuple
192h	0Ch	TPCE INDX	Configuration table index byte
194h	08h	TPCE FS	Features selection byte
196h	EAh	TPCE IO	I/O space information
198h	60h		
19Ah	40h		Address field (start of I/O address block) “0140h”
19Ch	01h		
19Eh	1Fh		Length field (Size: 32 byte)
200h	FFh		
202h	1Bh	CISTPL CE	Configuration entry tuple
204h	08h	TPL LINK	Pointer for next tuple
206h	0Dh	TPCE INDX	Configuration table index byte

Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 0Ch: Index 12					

Features selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

I/O space information

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

Configuration table index byte

7	6	5	4	3	2	1	0
Intfaec 0:	Default 0:	Configuration index 0Dh: Index 13					

Byte	Tuple ID	Tuple name	Description
208h	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

20Ah	EAh	TPCE IO	I/O space information

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

20Ch	60h		

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

20Eh	60h		Address field (start of I/O address block) “0160h”
210h	01h		
212h	1Fh		Length field (Size: 32 byte)
214h	FFh		
216h	1Bh	CISTPL CE	Configuration entry tuple
218h	08h	TPL LINK	Pointer for next tuple
21Ah	0Eh	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 0Eh: Index 14					

21Ch	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>21Eh</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>220h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>222h</td><td>80h</td><td></td><td>Address field (start of I/O address block) “0180h”</td></tr>
<tr><td>224h</td><td>01h</td><td></td><td></td></tr>
<tr><td>226h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>228h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>22Ah</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>22Ch</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>22Eh</td><td>0Fh</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
0Fh: Index 15</td></tr>
</table></td></tr>
<tr><td>230h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>232h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>234h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
</table>

Byte	Tuple ID	Tuple name	Description
236h	A0h		Address field (start of I/O address block) “01A0h”
238h	01h		
23Ah	1Fh		Length field (Size: 32 byte)
23Ch	FFh		
23Eh	1Bh	CISTPL CE	Configuration entry tuple
240h	08h	TPL LINK	Pointer for next tuple
244h	10h	TPCE INDX	Configuration table index byte
246h	08h	TPCE FS	Features selection byte
248h	EAh	TPCE IO	I/O space information
24Ah	60h		
24Ch	C0h		Address field (start of I/O address block) “0110h”
24Eh	01h		
250h	1Fh		Length field (Size: 32 byte)
252h	FFh		
254h	1Bh	CISTPL CE	Configuration entry tuple
256h	08h	TPL LINK	Pointer for next tuple
258h	11h	TPCE INDX	Configuration table index byte

TPCE INDX

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 10h: Index 16					

TPCE FS

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

TPCE IO

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

TPCE INDX

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 11h: Index 17					

Byte	Tuple ID	Tuple name	Description
25Ah	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

25Ch	EAh	TPCE IO	I/O space information
25Eh	60h		

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

260h	E0h		Address field (start of I/O address block) “01E0h”
262h	01h		
264h	1Fh		Length field (Size: 32 byte)
266h	FFh		
268h	1Bh	CISTPL CE	Configuration entry tuple
26Ah	08h	TPL LINK	Pointer for next tuple
26Ch	12h	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 12h: Index 18					

26Eh	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>270h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>272h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>274h</td><td>00h</td><td></td><td rowspan="2">Address field (start of I/O address block) “0200h”</td></tr>
<tr><td>276h</td><td>02h</td><td></td></tr>
<tr><td>278h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>27Ah</td><td>FFh</td><td></td><td></td></tr>
<tr><td>27Ch</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>27Eh</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>280h</td><td>13h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
13h: Index 19</td></tr>
</table></td></tr>
<tr><td>282h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>284h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>286h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>288h</td><td>20h</td><td></td><td>Address field (start of I/O address block) “0220h”</td></tr>
<tr><td>28Ah</td><td>02h</td><td></td><td></td></tr>
<tr><td>28Ch</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>28Eh</td><td>FFh</td><td></td><td></td></tr>
<tr><td>290h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>292h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>294h</td><td>14h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
14h: Index 20</td></tr>
</table></td></tr>
<tr><td>296h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>298h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>29Ah</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>29Ch</td><td>40h</td><td></td><td>Address field (start of I/O address block) “0240h”</td></tr>
<tr><td>29Eh</td><td>02h</td><td></td><td></td></tr>
<tr><td>2A0h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>2A2h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>2A4h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>2A6h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>2A8h</td><td>15h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
15h: Index 21</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>2AAh</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>2ACh</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>2AEh</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>2B0h</td><td>60h</td><td rowspan="2"></td><td rowspan="2">Address field (start of I/O address block) “0260h”</td></tr>
<tr><td>2B2h</td><td>02h</td></tr>
<tr><td>2B4h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>2B6h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>2B8h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>2BAh</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>2BCh</td><td>16h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
16h: Index 22</td></tr>
</table></td></tr>
<tr><td>2BEh</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>2C0h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>2C2h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>2C4h</td><td>80h</td><td></td><td>Address field (start of I/O address block) “0280h”</td></tr>
<tr><td>2C6h</td><td>02h</td><td></td><td></td></tr>
<tr><td>2C8h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>2CAh</td><td>FFh</td><td></td><td></td></tr>
<tr><td>2CCh</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>2CEh</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>2D0h</td><td>17h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
17h: Index 23</td></tr>
</table></td></tr>
<tr><td>2D2h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>2D4h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>2D6h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>2D8h</td><td>A0h</td><td></td><td>Address field (start of I/O address block) “02A0h”</td></tr>
<tr><td>2DAh</td><td>02h</td><td></td><td></td></tr>
<tr><td>2DCh</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>2DEh</td><td>FFh</td><td></td><td></td></tr>
<tr><td>2E0h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>2E2h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>2E4h</td><td>18h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
18h: Index 24</td></tr>
</table></td></tr>
<tr><td>2E6h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>2E8h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table>
I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>2ECh</td><td>C0h</td><td></td><td rowspan="2">Address field (start of I/O address block) “02C0”</td></tr>
<tr><td>2EEh</td><td>02h</td><td></td></tr>
<tr><td>2F0h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>2F2h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>2F4h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>2F6h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>2F8h</td><td>19h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
19h: Index 25</td></tr>
</table></td></tr>
<tr><td>2FAh</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>2FCh</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>2FEh</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>300h</td><td>E0h</td><td></td><td>Address field (start of I/O address block) “02E0h”</td></tr>
<tr><td>302h</td><td>02h</td><td></td><td></td></tr>
<tr><td>304h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>306h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>308h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>30Ah</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>30Ch</td><td>1Ah</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
1Ah: Index 26</td></tr>
</table></td></tr>
<tr><td>30Eh</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>310h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>312h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>314h</td><td>00h</td><td></td><td>Address field (start of I/O address block) “0300h”</td></tr>
<tr><td>316h</td><td>03h</td><td></td><td></td></tr>
<tr><td>318h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
</table>

Byte	Tuple ID	Tuple name	Description
31Ah	FFh		
31Ch	1Bh	CISTPL CE	Configuration entry tuple
31Eh	08h	TPL LINK	Pointer for next tuple
320h	1Bh	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 1Bh: Index 27					

322h	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

324h	EAh	TPCE IO	I/O space information

I/O space description byte

7	6	5	4	3	2	1	0
Range 1:	Bus 16 1:	Bus 8 1:	Number of I/O address lines 0Ah:				

326h	60h

I/O range description byte

7	6	5	4	3	2	1	0
Length field size 1: 1 byte		Address field size 2: 2 byte		Number of I/O ranges 0:			

328h	20h		Address field (start of I/O address block) “0320h”
32Ah	03h		
32Ch	1Fh		Length field (Size: 32 byte)
32Eh	FFh		
330h	1Bh	CISTPL CE	Configuration entry tuple
332h	08h	TPL LINK	Pointer for next tuple
334h	1Ch	TPCE INDX	Configuration table index byte

7	6	5	4	3	2	1	0
Intface 0:	Default 0:	Configuration index 1Ch: Index 28					

336h	08h	TPCE FS	Function selection byte

7	6	5	4	3	2	1	0
Miscella-neous 0:	Memory space 0:		IRQ 0:	IO space 1:	Timing 0:	Power 0: V_{CC}	

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>338h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>33Ah</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>33Ch</td><td>40h</td><td></td><td>Address field (start of I/O address block) “0340h”</td></tr>
<tr><td>33Eh</td><td>03h</td><td></td><td></td></tr>
<tr><td>340h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>342h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>344h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>346h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>348h</td><td>1Dh</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
1Dh: Index 29</td></tr>
</table></td></tr>
<tr><td>34Ah</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>34Ch</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>34Eh</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>350h</td><td>60h</td><td></td><td>Address field (start of I/O address block) “0360h”</td></tr>
<tr><td>352h</td><td>03h</td><td></td><td></td></tr>
<tr><td>354h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>356h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>358h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>35Ah</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>35Ch</td><td>1Eh</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
1Eh: Index 30</td></tr>
</table></td></tr>
<tr><td>35Eh</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>360h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table>
I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>362h</td><td>60h</td><td></td><td></td></tr>
<tr><td>364h</td><td>80h</td><td></td><td rowspan="2">Address field (start of I/O address block) “0380h”</td></tr>
<tr><td>366h</td><td>03h</td><td></td></tr>
<tr><td>368h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>36Ah</td><td>FFh</td><td></td><td></td></tr>
<tr><td>36Ch</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>36Eh</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>370h</td><td>1Fh</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
1Fh: Index 31</td></tr>
</table></td></tr>
<tr><td>372h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>374h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>376h</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>378h</td><td>A0h</td><td></td><td>Address field (start of I/O address block) “03A0h”</td></tr>
<tr><td>37Ah</td><td>03h</td><td></td><td></td></tr>
<tr><td>37Ch</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>37Eh</td><td>FFh</td><td></td><td></td></tr>
<tr><td>380h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>382h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>384h</td><td>20h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
20h: Index 32</td></tr>
</table></td></tr>
<tr><td>386h</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>388h</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table></td></tr>
<tr><td>38Ah</td><td>60h</td><td></td><td>I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>38Ch</td><td>C0h</td><td></td><td>Address field (start of I/O address block) “03C0h”</td></tr>
<tr><td>38Eh</td><td>03h</td><td></td><td></td></tr>
<tr><td>390h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
</table>

<table>
<tr><th>Byte</th><th>Tuple ID</th><th>Tuple name</th><th>Description</th></tr>
<tr><td>392h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>394h</td><td>1Bh</td><td>CISTPL CE</td><td>Configuration entry tuple</td></tr>
<tr><td>396h</td><td>08h</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>398h</td><td>21h</td><td>TPCE INDX</td><td>Configuration table index byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Intface
0:</td><td>Default
0:</td><td colspan="6">Configuration index
21h: Index 33</td></tr>
</table></td></tr>
<tr><td>39Ah</td><td>08h</td><td>TPCE FS</td><td>Function selection byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Miscella-
neous
0:</td><td colspan="2">Memory space
0:</td><td>IRQ
0:</td><td>IO space
1:</td><td>Timing
0:</td><td colspan="2">Power
0: V_{CC}</td></tr>
</table></td></tr>
<tr><td>39Ch</td><td>EAh</td><td>TPCE IO</td><td>I/O space information
I/O space description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Range
1:</td><td>Bus 16
1:</td><td>Bus 8
1:</td><td colspan="5">Number of I/O address lines
0Ah:</td></tr>
</table>
I/O range description byte
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">Length field size
1: 1 byte</td><td colspan="2">Address field size
2: 2 byte</td><td colspan="4">Number of I/O ranges
0:</td></tr>
</table></td></tr>
<tr><td>39Eh</td><td>60h</td><td></td><td></td></tr>
<tr><td>3A0h</td><td>E0h</td><td></td><td rowspan="2">Address field (start of I/O address block) “03E0h”</td></tr>
<tr><td>3A2h</td><td>03h</td><td></td></tr>
<tr><td>3A4h</td><td>1Fh</td><td></td><td>Length field (Size: 32 byte)</td></tr>
<tr><td>3A6h</td><td>FFh</td><td></td><td></td></tr>
<tr><td>3A8h</td><td>22h</td><td>CISTPL FUNCE</td><td></td></tr>
<tr><td>3AAh</td><td>0Ch</td><td>TPL LINK</td><td>Pointer for next tuple</td></tr>
<tr><td>3ACh</td><td>00h</td><td></td><td>Reserve</td></tr>
<tr><td>3AEh</td><td>01h</td><td>LAN TECH</td><td>10BASE-T Ethernet</td></tr>
<tr><td>3B0h</td><td>01h</td><td>LAN MEDIA</td><td></td></tr>
<tr><td>3B2h</td><td>04h</td><td>LAN CON</td><td></td></tr>
<tr><td>3B4h</td><td>06h</td><td>LAN ID SIZ</td><td>ID number byte size</td></tr>
</table>

Byte	Tuple ID	Tuple name	Description
3B6h	80h	NODE ID	
3B8h	02h		
3BAh	04h		
3BCh	06h		
3BEh	08h		
3C0h	0Ah		
3C2h	FFh	CISTPL END	Tuple link end tuple

Notes:
1. The contents of card information structure (CIS) are subject to change.
2. The contents of CIS can be changed upon user requests.

1.2 Card configuration register (CCR)

The system must write to the CCR where is specified by the configuration base address of the CIS.

The MBH10302 has four configuration registers: Configuration Option Register (CCOR), Card Configuration Register (CCSR), Pin Replacement Register (PRR), and Socket Copy Register (SCR). These registers are all writable and exist in the attribute memory space.

$\overline{CE1}$	$\overline{REG}$	$\overline{OE}$	$\overline{WE}$	A11 ——————— A0	Register selected	—
L	L	L	H	HHHHHHHHHHHLLLLL	CCOR READ	FFE0h
L	L	H	L		CCOR WRITE	
L	L	L	H	HHHHHHHHHHHLLLHL	CCSR READ	FFE2h
L	L	H	L		CCSR WRITE	
L	L	L	H	HHHHHHHHHHHLLHLL	PRR READ	FFE4h
L	L	H	L		PRR WRITE	
L	L	L	H	HHHHHHHHHHHLLHHL	SCR READ	FFE6h
L	L	H	L		SCR WRITE	

Note: The CCSR is cleared by the system hardware reset.

1.2.1 Configuration option register (CCOR)

The CCOR is for system configuration and program resetting. This register is a read/write register with three fields.

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	Lev1REQ	Configuration index					

The CCOR becomes 00h after resetting.

D7: SRESET	Setting this bit to 1 places the card in the reset state by clearing all configurations and control status registers. The reset state is the same as a hardware reset except that this bit cannot be reset. Returning this bit to 0 leaves the card in the reset state immediately after power-on (Default = 0).
D6: LvelREQ	A pulse or level mode interrupt is selected by an interrupt. – 0: Pulse mode – 1: Level mode With this bit signal, the card selects whether a pulse or level signal is output to the IRQ pin (Default = 0).
D5 to D0: Configuration index	This field selects one of the configuration entry tuple indices 0 to 33 in the card configuration table related to the configuration that the system is specified for the card (Default = 0).

1.2.2 Configuration status register (CCSR)

The CCSR is an optional register for storing data about the card status. The default is 00h.

D7	D6	D5	D4	D3	D2	D1	D0
Changed	SigChg	IOis8	Rsvd0	Audio	PwDwn	Intr	Rsvd0

D7: Changed	This bit indicates that one or more bits of the pin replacement registers (CBVD1, CBVD2, CRady/$\overline{\text{Bsy}}$, or CWprot) are set to 1. When a changed bit is set, the BVD1 pin is held at Low level when the SigChg bit is 1 and the card is configured (Default = 0).
D6: SigChg	This bit is set or reset by the system to enable or disable the status change signal ($\overline{\text{STSCHG}}$) from the status register. Setting this bit to 1 controls the $\overline{\text{STSCHG}}$ signal. If there is no mode for the $\overline{\text{STSCHG}}$ signal, this bit is set to 0 to keep the signal High level (Default = 0).
D5: IOis8	This bit supports both 8- and 16-bit I/O access. This bit is only read and is always negated (=0). Writing to this pin has no effect.
D4: Rsvd0	Reserved bit. This bit must be set to 0.
D3: Audio	This bit is not implemented and is always 0.
D2: PwDwn	When this bit is set to 1, the card starts the power-down mode. The card completes all pending processes (i.e. E^2PROM write) before starting the power-off sequence. The power-off process includes shutting down the LAN controller and transceiver IC.
D1: Intr	This bit indicates the interrupt request internal status. This bit is enabled whether or not interrupts are configured. When this bit is set to 1, interrupt is disabled. When it is set to 0, interrupt is enabled.
D0: Rsvd0	Reserved bit. This bit must be set to 0.

1.2.3 Pin replacement register (PRR)

The PRR is used for providing the state of the card connected to pins 16, 33, 62, and 63 on the IC memory card interface.

The PRR is a read/write register and serves as a mask to change the high-order four bits corresponding to the written low-order bits.

D7	D6	D5	D4	D3	D2	D1	D0
CBVD1	CBVD2	CRdy/$\overline{\text{Bsy}}$	CWProt	RBVD1	RBVD2	RRdy/$\overline{\text{Bsy}}$	RWProt

D7: CBVD1 D6: CBVD2	These bits must be 0.
D5: Crdy/$\overline{\text{Bsy}}$	This bit is set to 1 when the RRdy/$\overline{\text{Bsy}}$ bit is changed. This bit can be written by the system.. Writing to this bit occurs only when the following conditions are met: a. To write to bit D5, the system must set D1 to 1. If D1 is set to 0, no writing occurs. b. When D5 is set to 0, writing to D5 is not allowed, When D5 is set to 1, writing of both 1 and 0 is allowed. (This means that the system cannot accidentally introduce a status change that did not occur.)
D4: CWProt D3: RBVD1 D2: RVD2	These bits must be 0.
D1: RRdy/$\overline{\text{Bsy}}$	This bit indicates the internal status of the Ready/$\overline{\text{Busy}}$ signal. This bit is used to define the Ready or $\overline{\text{Busy}}$ status when the corresponding pins are assigned for interrupt request on the I/O card interface. When this bit is set to 1, the card is ready for the PCMCIA transaction.
D0: RWProt	This bit indicates the status of the write protect switch. This bit must be 0.

1.2.4 Socket copy register (SCR)

The SCR is an optional read/write register to use the card for identification between similar cards incorporated in the system. This register is always written before writing to the card configuration option register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Copy Number			Socket Number			

D7: Reserved	This bit is reserved for future standardization. This bit must be set to 0 by software when writing to the register.
D6 to D4: Copy number	A card may be indicated in the CIS to be configured with one or more cards. Such a card has a copy number which is described in the socket copy register by the system. This field indicates what copy version of the card is inserted in the system that is configured with each card. The Ethernet ignores this field.
D3 to D0: Socket number	This field indicates to the card which socket each card is inserted into. The Ethernet ignores this field.

2. I/O Mode Register

The I/O memory contains three address spaces. They are the Ethernet control registers, Ethernet Control registers, and the Ethernet ID number. The Ethernet supports JEIDA independent and overlapping I/O addressing mode. The MBH10302 has 34 I/O indexes. Index 1 is used for independent I/O addressing. Indexes 2 to 33 are reserved for overlapping I/O addressing. Index 0 is used to disable all I/O functions.

The Ethernet I/O address space is 32 bytes deep. In the independent I/O addressing mode, it is used only for address comparison. The MBH10302 expects the system to have each PCMCIA card slot with its own unique card enable signal (I/O address space). Systems that do not support this capability (i.e. ISA and EISA buses) must be used in the overlapping I/O addressing mode. In this mode, the 32-byte Ethernet I/O address space is assigned to one of the 32 possible preassigned I/O spaces. The system selects a different I/O base address to the configuration option register. Only addresses A9 to A0 are used for address comparison.

The mappings for Ethernet overlapping I/O addressing are defined as follows:

Index 0	I/O address space:	I/O Disabled
Index 1	I/O address space:	Independent I/O address
Index 2	I/O address space:	000h to 01Fh (I/O base address = 0)
Index 3	I/O address space:	020h to 03Fh (I/O base address = 20)
Index 4	I/O address space:	040h to 05Fh (I/O base address = 40)
Index 5	I/O address space:	060h to 07Fh (I/O base address = 60)
Index 6	I/O address space:	080h to 09Fh (I/O base address = 80)
Index 7	I/O address space:	0A0h to 0BFh (I/O base address = A0)
Index 8	I/O address space:	0C0h to 0DFh (I/O base address = C0)
Index 9	I/O address space:	1E0h to 0FFh (I/O base address = E0)
Index 10	I/O address space:	100h to 11Fh (I/O base address = 100)
Index 11	I/O address space:	120h to 13Fh (I/O base address = 120)
Index 12	I/O address space:	140h to 15Fh (I/O base address = 140)
Index 13	I/O address space:	160h to 17Fh (I/O base address = 160)
Index 14	I/O address space:	180h to 19Fh (I/O base address = 180)
Index 15	I/O address space:	1A0h to 1BFh (I/O base address = 1A0)
Index 16	I/O address space:	1C0h to 1DFh (I/O base address = 1C0)
Index 17	I/O address space:	1E0h to 1FFh (I/O base address = 1E0)
Index 18	I/O address space:	200h to 21Fh (I/O base address = 200)
Index 19	I/O address space:	220h to 23Fh (I/O base address = 220)
Index 20	I/O address space:	240h to 25Fh (I/O base address = 240)
Index 21	I/O address space:	260h to 27Fh (I/O base address = 260)
Index 22	I/O address space:	280h to 29Fh (I/O base address = 280)
Index 23	I/O address space:	2A0h to 2BFh (I/O base address = 2A0)
Index 24	I/O address space:	2C0h to 2DFh (I/O base address = 2C0)
Index 25	I/O address space:	2E0h to 2FFh (I/O base address = 2E0)
Index 26	I/O address space:	300h to 31Fh (I/O base address = 300)
Index 27	I/O address space:	320h to 33Fh (I/O base address = 320)
Index 28	I/O address space:	340h to 35Fh (I/O base address = 340)
Index 29	I/O address space:	360h to 37Fh (I/O base address = 360)
Index 30	I/O address space:	380h to 39Fh (I/O base address = 380)
Index 31	I/O address space:	3A0h to 3BFh (I/O base address = 3A0)
Index 32	I/O address space:	3C0h to 3DFh (I/O base address = 3C0)
Index 33	I/O address space:	3E0h to 3FFh (I/O base address = 3E0)

The LAN I/O address assignments for the LAN control registers, Ethernet control registers, and Ethernet ID number are as follows:

Base Address + 00h to 0Fh	Ethernet card control register
Base Address + 10h	LAN card control register
Base Address + 11h	LAN card status register
Base Address + 12h	LAN card test register 1
Base Address + 13h	LAN card test register 2
Base Address + 14h to 17h	Reserved
Base Address + 1Ah to 1Fh	Ethernet ID number

2.1 LAN Card Control Register (Base Address + 10h)

D7:	**E^{2}PROM Write Enable:** When this bit is set to 1, writing to the E^{2}PROM containing the attribute memory space and the Ethernet ID number is enabled. If this bit is 0, all writing to the E^{2}PROM is ignored. Default = 0.
D6:	**Link Integrity Check Interrupt Mask:** When this bit is set to 1, the MBH10302 generates an interrupt if the 10 BASE-T integrity check is failed. When this bit is 0, the integrity failure interrupt is masked and the interrupt output is negated. Default = 0.
D5:	**Jabber Status Interrupt Mask:** When this bit is set to 1, the MBH10302 card generates an interrupt if the 10 BASE-T interface enters the jabber status. When this bit is 0, the jabber status interrupt is masked and the interrupt output is invarid. Default = 0.
D4:	**LAN Controller Interrupt Mask:** When this bit is set to 1, interrupts generated by the LAN controller are transferred to the host CPU. When it is 0, the LAN controller interrupt is masked and the interrupt output is invalid. Default = 0.
D3:	**UTP:** When this bit is set to 1, the 10 BASE-T transceiver is set for unshielded twisted-pair cable. When it is 0, it is set for shielded twisted-pair cable. Default = 1.
D2:	**NTH:** When this bit is set to 1, the 10 BASE-T transceiver is programmed for normal twisted-pair squelch threshold. When it is 0, the squelch threshold is pull down by 4.5 dB. Default = 1.
D1:	**Transceiver Loop Back:** When this bit is set to 1, transmitted Ethernet data is looped-back at the 10 BASE-T transceiver. This is used for Ethernet diagnosis. This bit must be 0 for normal operation. Default = 1.
D0:	**Link Integrity Test Enable:** When this bit is set to 1, the 10 BASE-T link integrity test is enabled. If it is 0, the test is disabled. This bit should be set to 1 for normal operation. Default = 1.

2.2 LAN Card Status Register (Base Address + 11h)

D7 to 3:	Reserved
D2:	**LAN Controller Interrupt:** When this bit is set to 1, it indicates that an interrupt from the LAN controller has occurred. This bit is defaulted to 0 at power-on. This bit is read only. It is set to 0 when the interrupt condition has been serviced by the system.
D1:	**Jabber Interrupt Status:** When this bit is set to 1, it indicates that a jabber interrupt from the 10-BASE-T transceiver has occurred. This bit is defaulted to 0 at power-on. This bit is read only. It is set to 0 when the interrupt condition has been serviced by the system.
D0:	**Link Integrity Failure Interrupt:** When this bit is set to 1, it indicates that a link integrity failure from the 10-BASE-T transceiver has occurred. This bit is defaulted to 0 at power-on. This bit is read only. It is set to 0 when the interrupt condition has been serviced by the system.

2.3 LAN Card Test Registers 1 and 2 (Base Address + 12h and 13h)

D7 to 0:	These registers are used for system diagnosis. They allow the system to write and read test patterns from the Ethernet. During normal operation, all bits in these two registers must be 0.

2.4 Ethernet ID Number (Base Address + 1Ah to 1Fh)

D7 to 0:	I/O base address + 1Ah to 1Fh are the six bytes of the Ethernet ID number.

2.5 Ethernet Control Register (Base Address + 00 to 0F)

There are 32 Ethernet control registers which consist of I/O address space 00h to 0Fh and two address extension bits (RBNK0 and RBNK1). The two address extension bits (RBNK0 and RBNK1) reside at bits D1 and D0 of the configuration register (I/O address = base + 06). The address assignments are as follows:

Register	Register symbol	Address					Bank	
		A4	A3	A2	A1	A0	RBNK1	RBNK0
Transmit status register	DLCR0	1	0	0	0	0	×	×
Receive status register	DLCR1	1	0	0	0	1	×	×
Transmit mask register	DLCR2	1	0	0	1	0	×	×
Receive status register	DLCR3	1	0	0	1	1	×	×
Transmit mode register	DLCR4	1	0	1	0	0	×	×
Receive mode register	DLCR5	1	0	1	0	1	×	×
Configuration register 0	DLCR6	1	0	1	1	0	×	×
Configuration register 1	DLCR7	1	0	1	1	1	×	×
Node ID register 0	DLCR8	1	1	0	0	0	0	0
Node ID register 1	DLCR9	1	1	0	0	1	0	0
Node ID register 2	DLCR10	1	1	0	1	0	0	0
Node ID register 3	DLCR11	1	1	0	1	1	0	0
Node ID register 4	DLCR12	1	1	1	0	0	0	0
Node ID register 5	DLCR13	1	1	1	0	1	0	0
TDR register 0 (LSB)	DLCR14	1	1	1	1	0	0	0
TDR register 1 (MSB)	DLCR15	1	1	1	1	1	0	0
Multicast address register 0	MAR8	1	1	0	0	0	0	1
Multicast address register 1	MAR9	1	1	0	0	1	0	1
Multicast address register 2	MAR10	1	1	0	1	0	0	1
Multicast address register 3	MAR11	1	1	0	1	1	0	1
Multicast address register 4	MAR12	1	1	1	0	0	0	1
Multicast address register 5	MAR13	1	1	1	0	1	0	1
Multicast address register 6	MAR14	1	1	1	1	0	0	1
Multicast address register 7	MAR15	1	1	1	1	1	0	1
Transmit/receive buffer port register 0 (LSB)	BMPR8	1	1	0	0	0	1	0
Transmit/receive buffer port register 1 (MSB)	BMPR9	1	1	0	0	1	1	0
Transmit start register	BMPR10	1	1	0	1	0	1	0
16-collision control register	BMPR11	1	1	0	1	1	1	0
Reserved register	BMPR12	1	1	1	0	0	1	0
Unused (reserved register)	BMPR13	1	1	1	0	1	1	0
Received skip packet register	BMPR14	1	1	1	1	0	1	0
Reserved register	BMPR15	1	1	1	1	1	1	0

Notes:

1. The node ID (DLCR8 to DLCR13) and multicast address (MAR8 to MAR15) registers can be accessed for read and write only during card initialization (Bit 7 [–ENA DLC] of the DLCR6= 1).
2. The LAN controller is defaulted to the 8-bit system interface at reset. Only byte access can be used at the Ethernet controller registers until the LAN controller is configured as the 16-bit system interface. After the LAN controller is configured, both byte and word access are used at all Ethernet registers except the transmit/receive buffer port register 1 where only word access can be used.

Register	Register symbol	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Transmit status register	DLCR0	R	TMT OK	NET BSY	TMT REC	SRT PKT	0	COL	16 COL	BUS WR ERR
		W	BIT CLR	—	—	—	0	BIT CLR	BIT CLR	BIT CLR
Receive status register	DLCR1	R	PKT RDY	BUS RD ERR	DMA EOP	RMT RST	RX SRT ERR	ALG ERR	CRC ERR	OVRFLO
		W	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR
Transmit mask register	DLCR2	R	ENA TMT OK	0	ENA TMT REC	0	0	ENA COL	ENA 16 COL	ENA BUS WR ERR
		W		0		0	0			
Receive status register	DLCR3	R	ENA PKT RDY	ENA BUS RD ERR	ENA DMA EOP	ENA RMT RST	ENA RX RST PKT	ENA ALG ERR	ENA CRC ERR	ENA OVRFLO
		W								
Transmit mode register	DLCR4	R	COL3	COL2	COL1	COL0	TST1	–TM	–LBC	DSC
		W	—	—	—	—	0			
Receive mode register	DLCR5	R	TST2	BUF EMP	ACRT BAD PKT	ADD SIZE	ENA SRT PKT	ENA REM RST	AM1	AM0
		W	0	—						
Configuration register 0	DLCR6	R	–ENA DLC	100/ –150ns	SB/–SW	BB/–BW	TX BUF SIZE1	TX BUF SIZE0	BUF SIZE1	BUF SIZE0
		W								
Configuration register 1	DLCR7	R	EED CNTL1	EED CNTL0	–STBY	RDYPN SEL	RBNK1	RBNK0	EOP/ –EOP	BYTE SWAP
		W				—				
Node ID register 0	DLCR8	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		W								
Node ID register 1	DLCR9	R	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		W								
Node ID register 2	LDCR10	R	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
		W								
Node ID register 3	DLCR11	R	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
		W								
Node ID register 4	DLCR12	R	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
		W								
Node ID register 5	DLCR13	R	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
		W								
TDR register 1 (LSB)	DLCR14	R	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
		W	—	—	—	—	—	—	—	—

(Continued)

Register	Register symbol	R/W	D7	D6	D5	D4	D3	D2	D1	D0
TDR register 1 (MSB)	DLCR15	R	0	0	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8
		W	—	—	—	—	—	—	—	—
Multicast address register 0	MAR8	R	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
		W								
Multicast address register 1	MAR9	R	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
		W								
Multicast address register 2	MAR10	R	MID23	MID22	MID21	MID20	MID19	MID18	MID17	MID16
		W								
Multicast address register 3	MAR11	R	MID31	MID30	MID29	MID28	MID27	MID26	MID25	MID24
		W								
Multicast address register 4	MAR12	R	MID39	MID38	MID37	MID36	MID35	MID34	MID33	MID32
		W								
Multicast address register 5	MAR13	R	MID47	MID46	MID45	MID44	MID43	MID42	MID42	MID40
		W								
Multicast address register 6	MAR14	R	MID55	MID54	MID53	MID52	MID51	MID50	MID49	MID48
		W								
Multicast address register 7	MAR15	R	MID63	MID62	MID61	MID60	MID59	MID58	MID57	MID56
		W								
Transmit/receive buffer port register	BMPR8	R	BMP7	BMP6	BMP5	BMP4	BMP3	BMP2	BMP1	BMP0
		W								
		R	BMP15	BMP14	BMP13	BMP12	BMP11	BMP10	BMP9	BMP8
		W								
Transmit start register	BMPR10	R	0	TX PKT CNT6	TX PKT CNT5	TX PKT CNT4	TX PKT CNT3	TX PKT CNT2	TX PKT CNT1	TX PKT CNT0
		W	TMST							
16-collision control register	BMPR11	R	0	0	0	0	0	16 COL CNTL2	16 COL CNTL1	16 COL CNTL0
		W	—	—	—	—	—			
Reserved register	BMPR12	R	—	—	—	—	—	—	—	—
		W	0	0	0	0	0	0	0	0
Unused (reserved register)	BMPR13	R	—	—	—	—	—	—	—	—
		W	0	0	0	0	0	0	0	0
Received skip packet register	BMPR14	R	—	—	—	—	—	SKIP RX PKT	—	—
		W	0	0	0	0	0		0	0
Reserved register	BMPR15	R	—	—	—	—	—	—	—	—
		W	0	0	0	0	0	0	0	0

3. Data Link Control Registers

3.1 Transmit status register (DLCR0)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	TMT OK	NET BSY	TMT REC	SRT PKT	0	COL	16 COL	BUS WR ERR
Write	BIT CLR	—	—	—	0	BIT CLR	BIT CLR	BIT CLR
Initial value	0	Undefined	0	0	0	0	0	0

D	Symbol	Operation	Bit value	Description
7	TMT OK (transmit OK)	READ	0	Indicates transmit status
			1	This bit value is set automatically when all packets in the active transmit buffer have been successfully transmitted. In the single buffer mode, it indicates that the next data can be transmitted from the host CPU. In the dual buffer mode, it indicates that the second bank transmit can be active (Bit 7 [TMST] of the BMR10 is set). The dual buffer mode also allows the host CPU to transmit the next data to one buffer during packet transmission at another buffer.
		WRITE	0	No effect
			1	This bit is cleared.
6	NET BSY (net busy)	READ	0	Indicates that network empty (no carrier detected)
			1	Indicates that network in use (carrier detected)
		WRITE	—	No effect
5	TMT OK (transmit packet received)	READ	0	Indicates that transmit packet is not received properly. This bit is cleared automatically as each transmission begins.
			1	Indicates that transmit packet received properly. This bit need not be used for normal operation.
		WRITE	—	No effect
4	SRT PKT (short packet)	READ	0	Short packet has no error. This bit is cleared automatically as each transmission begins.
			1	Indicates that carrier on network field disappeared during packet transmission. This bit is usually set by a collision or physical cable fault.
		WRITE	—	No effect
3	Reserved	READ	—	always read data ”0”
		WRITE	—	always written data ”0”
2	COL (collision error)	READ	0	No collision error
			1	Indicates that packet collision occurred on network during transmission. The data controller automatically retransmits the packet after up to 15 collisions. The number of collisions can be read at Bit 7 of the DLCR4 (collision register counter).
		WRITE	0	No effect
			1	This bit is cleared.

Bit	Symbol	Operation	Bit value	Description
1	16 COL (16-collision error)	READ	0	No 16-collision error
			1	Indicates that 16 consecutive collisions occurred during packet transmission. Operation after 16 collision errors can be set by Bits 2 and 1 of the BMPR11 (16-collision control register).
		WRITE	0	No effect
			1	This bit is cleared.
0	BUS WR ERR (bus write error)	READ	0	No bus write error
			1	Indicates that RDY signal cannot be asserted within 2.4 µs when host CPU writes transmit data to transmit buffer. No transmit data is written because the transmit buffer is full. This bit is not set during transmission according to the normal operation flow.
		WRITE	0	No effect
			1	This bit is cleared.

3.2 Receive status register (DLCR1)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	PKT RDY	BUS RD ERR	DMA EOP	RMT RST	RX SRT PKT	ALG ERR	CRC ERR	OVRFLO
Write	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR
Initial value	0	0	0	0	0	0	0	0

D	Symbol	Operation	Bit value	Description
7	PKT RDY (packet ready)	READ	0	No received packet stored in receive buffer
			1	Indicates that packet properly is received and stored in receive buffer. There is at least one received packet in the receive buffer.
		WRITE	0	No effect
			1	This bit is cleared. However, if any received packet still remains in the receive buffer after the host CPU reads one received packet from the receive buffer, this bit is automatically set.
6	BUS RD ERR (bus read error)	READ	0	No bus read error occurs
			1	Indicates that signal RDY cannot be asserted within 2.4 µs when host CPU reads data in received buffer. The host CPU tried to read the receive buffer despite there being no data to transmit in the buffer.
		WRITE	0	No effect
			1	This bit is cleared.
5	DMA EOP	READ	—	Indicates DMA transfer. This function is not used in the MBH10302.
		WRITE	0	No effect
			1	This bit is cleared. Writing 1 at this bit is inhibited.

D	Symbol	Operation	Bit value	Description
4	RMT RST (remote reset)	READ	0	The received packet is not a remote reset packet.
			1	Indicates that data length field of received packet is 0900H. This bit is set when Bit 2 (ENA RMT RST) of the DLCR5 is set and the physical addresses are met. This bit is not set for multi-cast and broadcast addresses.
		WRITE	0	No effect
			1	This bit is cleared. This bit is automatically cleared at the start of the next receive packet.
3	RX SRT PKT (short packet)	READ	0	No short packet error
			1	Indicates that data length of received packet (address + data length + data) does not meet specified minimum data length (60 bytes). If Bit 3 (ENA SRT PKT) of the DLCR5 is set, this bit is set when the received data length is less than 6 bytes.
		WRITE	0	No effect
			1	This bit is cleared.
2	ALG ERR (alignment error)	READ	0	No alignment error
			1	Indicates that CRC of received packet not correct and bit count of received data does not exceed multiple of 8
		WRITE	0	No effect
			1	This bit is cleared.
1	CRC ERR (CRC error)	READ	0	No CRC error
			1	Indicates that CRC of received packet not correct
		WRITE	0	No effect
			1	This bit is cleared.
0	OVRFLO (overflow error)	READ	0	No overflow error
			1	Indicates that received packet exceeding free space of received buffer is deleted. If the next packet is less than the free space of the received buffer, the packet data is received properly even when this bit is set. If this bit is set, the buffer is full. Transfer the received buffer data to the host CPU immediately.
		WRITE	0	No effect
			1	This bit is cleared.

3.3 Transmit mask register (DLCR2)

	D7	D6	D5	D4	D3	D2	D1	D0
Read/ Write	ENA TMT OK	0	ENA TMT REC	0	0	ENA COL	ENA 16COL	ENA BUS WR ERR
Initial value	0	0	0	0	0	0	0	0

D	Symbol	Operation	Bit value	Description
7	ENA TMT OK	READ/ WRITE	0	TMT OK interrupt disabled
			1	TMT OK interrupt enabled
6	Unused	READ/ WRITE	—	”0” is always read. Always write ”0”.
5	ENA TMT REC	READ/ WRITE	0	TMT REC interrupt disabled
			1	TMT REC interrupt enabled
4, 3	Unused	READ/ WRITE	—	”0” is always read. Always write ”0”.
2	ENA COL	READ/ WRITE	0	COL interrupt disabled
			1	COL interrupt enabled
1	ENA 16COL	READ/ WRITE	0	16COL interrupt disabled
			1	16COL interrupt enabled
0	ENA BUS WR ERR	READ/ WRITE	0	ENA WR ERR interrupt disabled
			1	ENA WR ERR interrupt enabled

3.4 Receive mask register (DLCR3)

	D7	D6	D5	D4	D3	D2	D1	D0
Read/ Write	ENA PKT RDY	ENA BUS RD ERR	0	ENA RMT RST	ENA RX RMT PKT	ENA ALG ERR	ENA CRC ERR	ENA OVRFLO
Initial value	0	0	0	0	0	0	0	0

D	Symbol	Operation	Bit value	Description
7	ENA PKT RDY	READ/ WRITE	0	PKT RDY interrupt disabled
			1	PKT RDY interrupt enabled
6	ENA BUS RD ERR	READ/ WRITE	0	BUS RD ERR interrupt disabled
			1	BUS RD ER interrupt enabled
5	Unused	READ/ WRITE	—	”0” is always read. Always write ”0”.
4	ENA RMT RST	READ/ WRITE	0	RMT RST interrupt disabled
			1	RMT RST interrupt enabled
3	ENA RX RST ERR	READ/ WRITE	0	RX RST interrupt disabled
			1	RX RST interrupt enabled
2	ENA ALG ERR	READ/ WRITE	0	ALG ERR interrupt disabled
			1	ALG ERR interrupt enabled
1	ENA CRC ERR	READ/ WRITE	0	CRC ERR interrupt disabled
			1	CRC ERR interrupt enabled
0	ENA OVRFLO	READ/ WRITE	0	OVRFLO interrupt disabled
			1	OVRFLO interrupt enabled

3.5 Transmit mode register (DLCR4)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	COL3	COL2	COL1	COL0	TST1	–TM	–LBC	DSC
Write	—	—	—	—	0			
Initial value	—	—	—	—	0	1	1	0

D	Symbol	Operation	Bit value	Description
7 to 4	COL3 to COL0 (collision count)	READ	—	This bit is cleared at each start of packet transmission. It indicates the number of collisions until the transmission is completed
3	TST1 (chip test)	READ/ WRITE	—	Chip test bit. Always write 0 when writing to the DLCR4. Do not write 1 to this bit during normal operation.
2	–TM (test mode)	READ	1	”1” is always read.
		WRITE	—	Writing “0” to this bit is inhibited. Always write ”1”.
1	–LBC (loopback control)	READ/ WRITE	—	When this bit is set to ”0”, the LAN controller enters the loopback mode.
0	DSC (disable carrier detect)	READ/ WRITE	—	When this bit is set to 1, the transmitter of the data link controller becomes XCD. The carrier signal is ignored. This function is not used for normal Ethernet.

3.6 Receive mode register (DLCR5)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	TST2	BUF EMP	ACPT BAD PKG	ADD SIZE	ENA SRT PKT	ENA RMT RST	AM1	AM0
Write	0	—						
Initial value	0	1	0	0	0	0	0	

D	Symbol	Operation	Bit value	Description
7	TST2 (chip test)	READ/ WRITE	—	Chip test bit. Always write ”0” when writing to the DLCR5. Do not write ”1” to this bit during normal operation.
6	BUF EMP (buffer empty)	READ	0	Indicates that valid data remains in receive buffer
			1	Indicates that no valid data remains in receive buffer
		WRITE	—	No effect
5	ACRT BAD PKT (bad packet received)	READ/ WRITE	0	Received packet with short packet, alignment, or CRC errors is discarded and not transferred to receive buffer
			1	Packet with short packet, alignment, or CRC errors is transferred to receive buffer as normally-received packet
4	ADD SIZE (address size)	READ/ WRITE	0	Compares destination addresses of received packet and corresponding node IDs if all bytes (48 bits) agree
			1	Compares destination addresses of received packet and corresponding node IDs if high-order 5 bytes (40 bits) agree

<table>
<tr><th>D</th><th>Symbol</th><th>Operation</th><th>Bit value</th><th>Description</th></tr>
<tr><td rowspan="2">3</td><td rowspan="2">ENA SRT PKT (enable short packet)</td><td rowspan="2">READ/ WRITE</td><td>0</td><td>Packet with more than 60 bytes and less than 2 Kbytes can be received</td></tr>
<tr><td>1</td><td>Packet with more than 6 bytes and less than 2 Kbytes can be received</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">ENA RMT RST (enable remote reset)</td><td rowspan="2">READ/ WRITE</td><td>0</td><td>No remote set packet is detected</td></tr>
<tr><td>1</td><td>Checks that data field length of received packet is ”0900h”</td></tr>
<tr><td>1, 0</td><td>AM1, AM0 (address match mode)</td><td>READ/ WRITE</td><td>—</td><td>Selects destination address matching detection mode for receiving packets
<table>
<tr><th>AM1</th><th>AM0</th><th>Address Matching Detection Mode</th></tr>
<tr><td>0</td><td>0</td><td>No packet received. All packets are rejected as unmatched address.</td></tr>
<tr><td>0</td><td>1</td><td>Packet received with physical, broadcast, and multicast address, and low-order byte (three bytes from beginning of packet) matching corresponding node IDs.*</td></tr>
<tr><td>1</td><td>0</td><td>Packet received with physical, broadcast, and multicast address, and selected by multicast address.*</td></tr>
<tr><td>1</td><td>1</td><td>Any packet received irrespective of destination address</td></tr>
</table>
* The MBH10302 does not receive any broadcast and multicast packets that are sent by themselves, as well as any multicast packet that is sent by itself in the loopback mode.</td></tr>
</table>

3.7 Configuration register 0 (DLCR6)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	–ENA DLC	100 ns/–150 ns	SB/–SW	BB/–BW	TX BUF SIZE 1	TX BUF SIZE 0	BUF SIZE 1	BUF SIZE 0
Write		1					1	0
Initial value	1	0	1	1	0	1	1	0

<table>
<tr><th>D</th><th>Symbol</th><th>Operation</th><th>Bit value</th><th>Description</th></tr>
<tr><td>7</td><td>–ENA DLC (enable data link controller)</td><td>READ/ WRITE</td><td>0</td><td>Setting this bit to ”0” enables the MBH10302 to transmit/receive. When this bit is ”0”, the node ID and multicast registers cannot be accessed.</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>The data link controller and buffer manager of the MBH10302 are initialized and both the transmit and receive buffers are in the initial status.</td></tr>
<tr><td>6</td><td>100NS/–150NS (SRAM cycle time selection)</td><td>READ/ WRITE</td><td>—</td><td>SRAM cycle time selection bit. Always write ”1” when writing to the DLCR6. Do not write ”0” to this bit during normal operation.</td></tr>
<tr><td>5, 4</td><td>SB/–SW (system bus width selection)

BB/–BW (buffer memory bus width selection)</td><td>READ/ WRITE</td><td>—</td><td>Selects data bus width of system and buffer memory
<table>
<tr><th>SB/–SW</th><th>BB/–BW</th><th>System data bus</th><th>Buffer data bus</th></tr>
<tr><td>0</td><td>0</td><td colspan="2">Cannot be set</td></tr>
<tr><td>0</td><td>1</td><td>16 bits</td><td>8 bits</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Cannot be set</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Cannot be set</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>D</th><th>Symbol</th><th>Operation</th><th>Bit value</th><th>Description</th></tr>
<tr><td>3, 2</td><td>TX BUF SIZE1/
TX BUF SIZE0
(transmit buffer size)</td><td>READ/
WRITE</td><td>—</td><td>Transfers transmit buffer size
<table>
<tr><th colspan="2">TX BUF SIZE</th><th rowspan="2">Bank capacity</th><th rowspan="2">Number of banks</th><th rowspan="2">Buffer capacity</th></tr>
<tr><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>2 Kbytes</td><td>1</td><td>2 Kbytes</td></tr>
<tr><td>0</td><td>1</td><td>2 Kbytes</td><td>2</td><td>4 Kbytes</td></tr>
<tr><td>1</td><td>0</td><td>4 Kbytes</td><td>2</td><td>8 Kbytes</td></tr>
<tr><td>1</td><td>1</td><td>8 Kbytes</td><td>2</td><td>16 Kbytes</td></tr>
</table></td></tr>
<tr><td>1</td><td>BUF SIZE 1</td><td>READ/
WRITE</td><td>—</td><td>Buffer size selection bit. Always write ”1” when writing to the DLCR6. Do not write ”0” to this bit during normal operation.</td></tr>
<tr><td>0</td><td>BUF SIZE 0</td><td>READ/
WRITE</td><td>—</td><td>Buffer size selection bit. Always write ”0” when writing to the DLCR6. Do not write ”1” to this bit during normal operation.</td></tr>
</table>

3.8 Configuration register 1 (DLCR7)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	EDD CNTL 1	EDD CNTL 0	–STBY	RDYPNSEL	RBNK1	RBNK0	0	BYTE SWAP
Write	1	0		—				
Initial value	0	0	1	—	0	0	0	0

D	Symbol	Operation	Bit value	Description
7	EDD CNTL1	READ/ WRITE	—	LAN controller operation mode selection bit. Always write ”1” when writing to DLCR7. Do not write ”0” to this bit during operation.
6	EDD CNTL0	READ/ WRITE	—	LAN controller operation mode selection bit. Always write ”0” when writing to DLCR7. Do not write ”1” to this bit during operation.
5	–STBY	READ/ WRITE	0	Used to set controller to standby mode. The power consumption is reduced to one-seventh in the standby mode. To set the standby mode, initialize the controller by setting Bit 7 (–ENA DLC) of DLCR6 and then clear this bit.
			1	Operation status (not standby). To release the standby mode, reset the initial settings after setting this bit.
4	RDYPNSEL	READ	—	”0” is always read.
		WRITE	—	No effect

<table>
<tr><th>D</th><th>Symbol</th><th>Operation</th><th>Bit value</th><th>Description</th></tr>
<tr><td>3, 2</td><td>RBNK 1
RBNK 0</td><td>READ/
WRITE</td><td>—</td><td>The controller has three internal sets of registers. Switching bank by this bit enables access to each register set. DLCR0 to DLCR7 are accessible irrespective of the register bank.
<table>
<tr><th>RBNK 1</th><th>RBNK 0</th><th>Address = 00H to 07H</th><th>Address = 08H to 0FH</th></tr>
<tr><td>0</td><td>0</td><td>DLCR0 to DLCR7</td><td>DLCR8 to DLCR15</td></tr>
<tr><td>0</td><td>1</td><td>DLCR0 to DLCR7</td><td>MAR8 to MAR15</td></tr>
<tr><td>1</td><td>0</td><td>DLCR0 to DLCR7</td><td>BMPR8 to BMPR15</td></tr>
<tr><td>1</td><td>1</td><td>DLCR0 to DLCR7</td><td>BMPR8 to BMPR15</td></tr>
</table></td></tr>
<tr><td>1</td><td>Unused</td><td>READ/
WRITE</td><td>—</td><td>”0” is always read. Always write ”0” when writing to this bit.</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BYTE SWAP</td><td rowspan="2">READ/
WRITE</td><td>0</td><td>When the system bus is in the 16-bit mode, bytes are not swapped for accessing the BMPR8. This function responds to the Intel-type 16-bit bus.</td></tr>
<tr><td>1</td><td>When the system bus is in the 16-bit mode, high- and low-order bytes are swapped for accessing the BMPR8. This function responds to the Motorola-type 16-bit bus.</td></tr>
</table>

3.9 Node ID registers (DLCR8 to DLCR13)

	D7	D6	D5	D4	D3	D2	D1	D0
DLCR8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
DLCR9	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
DLCR10	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
DLCR11	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
DLCR12	ID39	ID38	ID27	ID36	ID35	ID34	ID33	ID32
DLCR13	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

The registers DLCR8 to DLCR13 store node IDs. After comparing the destination address of the received packet and these register values, a matching packet is received according to address match mode of DLCR5.

Set Bit 0 (ID 0) of DLCR8 to 0 normally. (The multicast address mode is set when Bit 0 of the destination address is 1. Therefore, a packet is received according to the setting of the address match mode bit of DLCR5 irrespective of the node ID in this register.)

The initial values of these registers are undefined. Read/write operation is possible only when Bit 7 (–ENA DLC) of DLCR6 is 1.

3.10 TDR registers (DLCR14 and 15)

	D7	D6	D5	D4	D3	D2	D1	D0
DLCR14	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
DLCR15	0	0	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

The registers DLCR14 and 15 are 14-bit counters that are reset at the start of transmission and count the number of transmit bits until a collision or carrier drop occurs.

These registers can only be read. Bits 7 and 6 of DLCR15 are always 0.

If any physical network failure such as an open circuit or short-circuit occurs, the values of these counters can give the approximate distance to the failure point. One count indicates 12 m (velocity of light $\times$ 0.8 $\times$ 100 ns $\times$ 0.5).

4. Multicast address registers (MAR8 to MAR15)

	D7	D6	D5	D4	D3	D2	D1	D0
MAR8	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
MAR9	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
MAR10	MID23	MID22	MID21	MID20	MID19	MID18	MID17	MID16
MAR11	MID31	MID30	MID29	MID28	MID27	MID26	MID25	MID24
MAR12	MID39	MID38	MID27	MID36	MID35	MID34	MID33	MID32
MAR13	MID47	MID46	MID45	MID44	MID43	MID42	MID41	MID40
MAR14	MID55	MID54	MID53	MID52	MID51	MID50	MID49	MID48
MAR15	MID63	MID62	MID61	MID60	MID59	MID58	MID57	MID56

These registers select the multicast address packet to receive when the address match mode bit of DLCR5 is set to 1 or 0. The multicast addresses are input to the 32-bit CRC circuit and are grouped into 64 groups according to the low-order 6 bits of the calculated CRC. Of these, packets with the multicast address of the group whose corresponding bit is set in these registers can be received.

The initial values of these registers are undefined. Read/write operation is possible only when Bit 7 (–ENA DLC) of DLCR6 is 1.

5. Buffer memory port registers

5.1 Transmit/receive buffer memory port register (BMPR8)

	D7	D6	D5	D4	D3	D2	D1	D0
BMPR8	BMP7	BMP6	BMP5	BMP4	BMP3	BMP2	BMP1	BMP0
	BMP15	BMP14	BMP13	BMP12	BMP11	BMP10	BMP9	BMP8

This register is a data port to transmit/receive data between the host system and the buffer memory. When the system interface is in the byte or 16-bit modes, this register is an 8- or 16-bit I/O port, respectively. In the 16-bit mode, this register can only handle word access while other registers can handle both word and byte access.

Moreover, the byte orders of the MSB and LSB of this register can be swapped by setting Bit 0 (BYTE SWAP) of DLCR7 to the 16-bit mode.

5.2 Transmit start register (BMPR10)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	TK PKT CNT 6	TK PKT CNT 5	TK PKT CNT 4	TK PKT CNT 3	TK PKT CNT 2	TK PKT CNT 1	TK PKT CNT 0
Write	TMST							
Initial value	0	0	0	0	0	0	0	0

D	Symbol	Operation	Bit value	Description
7	TMST	READ	0	Always set 0.
		WRITE	0	No effect
			1	Starts transmitting packet. If the transmit buffer is in the single buffer mode, set this bit after transferring the transmit packet from the host CPU to the transmit buffer. In the dual buffer mode, set this bit after transfer is ended (TMT OK bit of DLCR0 is set).
6 to 0	TX PKT CNT 0 to 6	READ	—	After starting packet transmission, the number of remaining packets are indicated by decrementing at the end of each packet transmission. When all packets are sent, these bits are 00H.
		WRITE	—	The controller can start multiple packet transmissions with one transmit command at a time. Write the number of transmit packets (transferred to buffer memory) to this register at the same time as setting the TMST bit.

5.3 16-collision control register (BMPR11)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	0	0	16COL CNTL 2	16COL CNTL 1	16COL CNTL 0
Write	0	0	0	0	0			
Initial value	0	0	0	0	0	0	0	0

D	Symbol	Operation	Bit value	Description
7 to 3	Unused	READ	0	Always set 0.
		WRITE	—	Do not write 1. Always write 0 when writing to this bit.
2 to 0	16COL CNTL 2 to 0	READ/ WRITE	—	See tables below.

16COL CNTL			Operation after 16 collisions
2	1	0	
1	1	0	The transmit packet that collided 16 times is automatically re-transmitted like general collision (Auto mode).
1	1	1	The transmit packet that collided 16 times is skipped and the next packet is transmitted (Auto mode).
0	1	×	When 16 collisions occur, the data link controller stops. To restart transmission, set the data in this register as shown in the following table. These data are valid only for restart. If the data link controller stops again as a result of 16 collisions, reset the following data to restart (Manual mode).

16COL CNTL			Restart of transmission in manual mode
2	1	0	
0	1	0	The transmit packet that collided 16 times is re-transmitted like general collision.
0	1	1	The transmit packet that collided 16 times is skipped and the next packet is transmitted.

5.4 Reserved register (BMPR12)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	—	—	—	—	—	—	—	—
Write	0	0	0	0	0	0	0	0
Initial value	—	—	—	—	—	—	—	—

D	Symbol	Operation	Bit value	Description
7 to 0	Unused	READ	0	The read value is always undefined.
		WRITE	—	Do not write 1. Always write 0 when writing to this bit.

5.5 Unused register (BMPR13)

	D7	D6	D5	D4	D3	D2	D1	D0
Read/ Write	—	—	—	—	—	—	—	—
Initial value	—	—	—	—	—	—	—	—

D	Symbol	Operation	Bit value	Description
7 to 0	Unused	READ	0	The read value is always undefined.
		WRITE	—	Do not write 1. Always write 0 when writing to this bit.

5.6 Receive skip packet register (BMPR14)

	D7	D6	D5	D4	D3	D2	D1	D0
Read/ Write	—	—	—	—	—	SKIP RX PKT	—	—
Initial value	—	—	—	—	—	0	—	—

D	Symbol	Operation	Bit value	Description
7 to 3, 1, 0	Unused	READ	0	The read value is always undefined.
		WRITE	—	Do not write 1. Always write 0 when writing to this bit.

D	Symbol	Operation	Bit value	Description
2	SKIP RX PKT	READ	0	Receive buffer pointer is not skipped
			1	Receive buffer pointer is skipped (updating). It indicates that operation is in a transient status after writing 1 to this bit until pointer skipping ends (within 320 ns).
		WRITE	0	No effect. The receive buffer pointer is not skipped.
			1	The receive buffer pointer is skipped to the head of the next packet by writing 1 to this bit. When the skip operation ends, this bit is automatically cleared. If the packet to be skipped is the last one in the receive buffer, the BUF EMP bit of DLCR5 is set after skipping the packet. Do not use this function until receive data is read more than four times (4 bytes in 8-bit bus mode or 4 words in 16-bit bus mode) and when the remaining receive data in the receive buffer is less than 8 bytes.

5.7 Reserved register (BMPR15)

	D7	D6	D5	D4	D3	D2	D1	D0
Read	—	—	—	—	—	—	—	—
Write								
Initial value	—	—	—	—	—	—	—	—

D	Symbol	Operation	Bit value	Description
7 to 0	Unused	READ	0	The read value is always undefined.
		WRITE	—	Do not write 1. Always write 0 when writing to this bit.

6. Common Memory

The Ethernet common memory is used for the emulate memory map function. The Ethernet receive/transmit buffer has two access ports. These are accessed via a normal I/O address space or a common memory space along with other Ethernet control registers. When accessing via the common memory space, the system must define a 32K address space in the common memory. This address space points to the receive/transmit buffer (emulate memory map). In other words, all read/write accesses are done directly to the receive/transmit buffer of the LAN controller in the 32K address space irrespective of these addresses.

The common memory address space starts from card address 0 which is defined by the card description tuple.

7. Ethernet Card E^2PROM

The LAN card has a 2K × 8 E^2PROM which is mapped only at even addresses 0 to 4K (000h to FFEh) of the attribute memory.

Writing the E^2PROM takes 100 µs to 10 ms. The LAN card contains a self-timer wite circuit and sets the Ready/Busy bit of the pin replacement resister to 0 when writing data. System access is limited to the four JEIDA configurations and the four LAN card control registers during write operation. Any location access is not allowed to the LAN cotrol register or other E^2PROMs. The LAN card is expected to check the Ready/Busy bit when E^2PROM write cycle is ended.

Absolute Maximum Rating

(Voltage referenced to GND)

Parameter	Symbol	Conditions	Ratings	Unit
Power voltage	V_{CC}		+6.0	V
Input voltage	V_{IN}	at 68-pin connector	GND – 0.5 to V_{CC} + 0.5	V
Operating temperature	PD		1500	mW
Power consumption	Topt		–10 to 70	°C

Recommended Operating Conditions

(Voltage referenced to GND)

Parameter	Symbol	Conditions	Recommended values			Unit
			Min.	Typical	Max.	
Power voltage	V_{CC}		4.75	5.0	5.25	V
	GND		—	0	—	V
Operating temperature	Topt		0	—	55	°C

Electrical Characteristics

(1) DC characteristics

• I/O interface

(Ta = 0° to 55°C, V_{CC} = 5.0 ±5%)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typical	Max.	
Power voltage	I_{SB}	At power down	—	60	—	mA
	I_{CC}	During transmission	—	180	260	mA
High level input voltage	V_{IH}		V_{CC} × 0.7	—	V_{CC}	V
Low level input voltage	V_{IL}		GND	—	V_{CC} × 0.3	V
High level output voltage	V_{OH}	I OH = –2 mA	4.0	—	V_{CC}	V
Low level output voltage	V_{OL}	I OL = 3.2 mA	—	—	0.4	V
Three-state leakage current	I_{OL}	VI = V_{CC} = GND	–10	—	10	μA

• **Transceiver interface**

(Ta = 0° to 55°C, V_{CC} = 5.0 ±5%)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typical	Max.	
Transmit output impedance	ZOUT		—	5	—	Ω
Peak output of differential voltage	V_{DD}	When loaded at 100 Ω	—	3.5	–2	V
Transmission jitter	—	Transmission filter output, line length: 0	—	—	±8	ns
		Transmission filter output 10 BASE–T is for a line model.	—	—	±3.5	ns
Receive input impedance	ZIN	Between TD+ and TD	—	20	—	KΩ
Differential voltage squelch level	V_{DS}		—	420	—	mV
Squelch level (at Low level)	V_{DSR}		—	300	—	mV
Receive jitter	—		—	—	1.5	ns

(2) AC characteristics

• **Jabber timing**

(Ta = 0° to 55°C, V_{CC} = 5.0 ±5%)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typical	Max.	
Maximum transmission time	t_1		20	—	150	ms
Jabber stop timer	t_2		250	—	750	ms

• **Link test timing**

(Ta = 0° to 55°C, V_{CC} = 5.0 ±5%)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typical	Max.	
Link loss time	t_1		55	—	66	ms
Link pulse cycle	t_2		8	—	24	ms
Regular link pulse receive pulse	t_3		4.1	—	65	ms

• **General timing**

(Ta = 0° to 55°C, V_{CC} = 5.0 ±5%)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typical	Max.	
Delay time to start reception	t_1		0	—	500	ns
Delay time to start transmission	t_2		0	—	200	ns
Delay time to start loopback	t_3		0	—	500	ns

TIMING

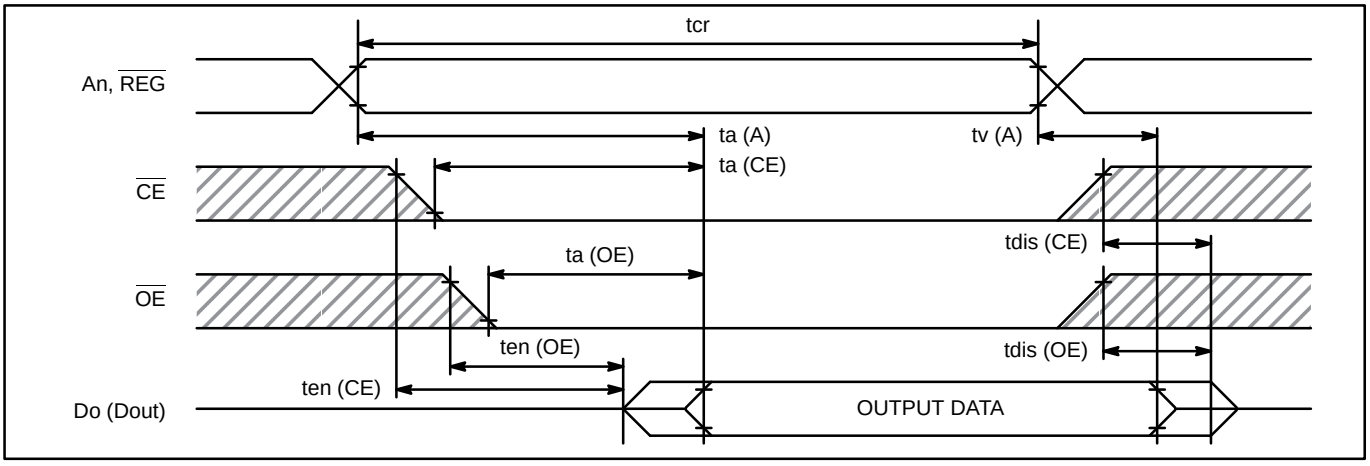
1. Attribute memory read timing

(1) Read timing specifications

Parameter		Symbol	Min.	Max.	Unit
Read cycle time		tcr	300	—	ns
Address access time		ta (A)	—	300	ns
$\overline{CE}$ access time		ta (CE)	—	300	ns
$\overline{OE}$ access time		ta (OE)	—	150	ns
Output disable time (CE)		tdis (CE)	—	100	ns
Output disable time (OE)		tdis (OE)	—	100	ns
Output enable time (CE)		ten (CE)	5	—	ns
Output enable time (OE)		ten (OE)	5	—	ns
Data effective time (A)		tv (A)	0	—	ns
Address set-up time	(Note 1)	tsu (A)	100	—	ns
Address hold time	(Note 1)	th (A)	20	—	ns
$\overline{CE}$ set-up time	(Note 1)	tsu (CE)	0	—	ns
$\overline{CE}$ hold time	(Note 1)	th (CE)	20	—	ns
Wait verification time ($\overline{CE}$)	(Note 1)	tv (WT-OE)	—	100	ns
Wait pulse width	(Note 2)	tw (WT)	—	12	µs
Data set-up time ($\overline{WAIT}$)	(Note 2)	tv (WT)	0	—	ns

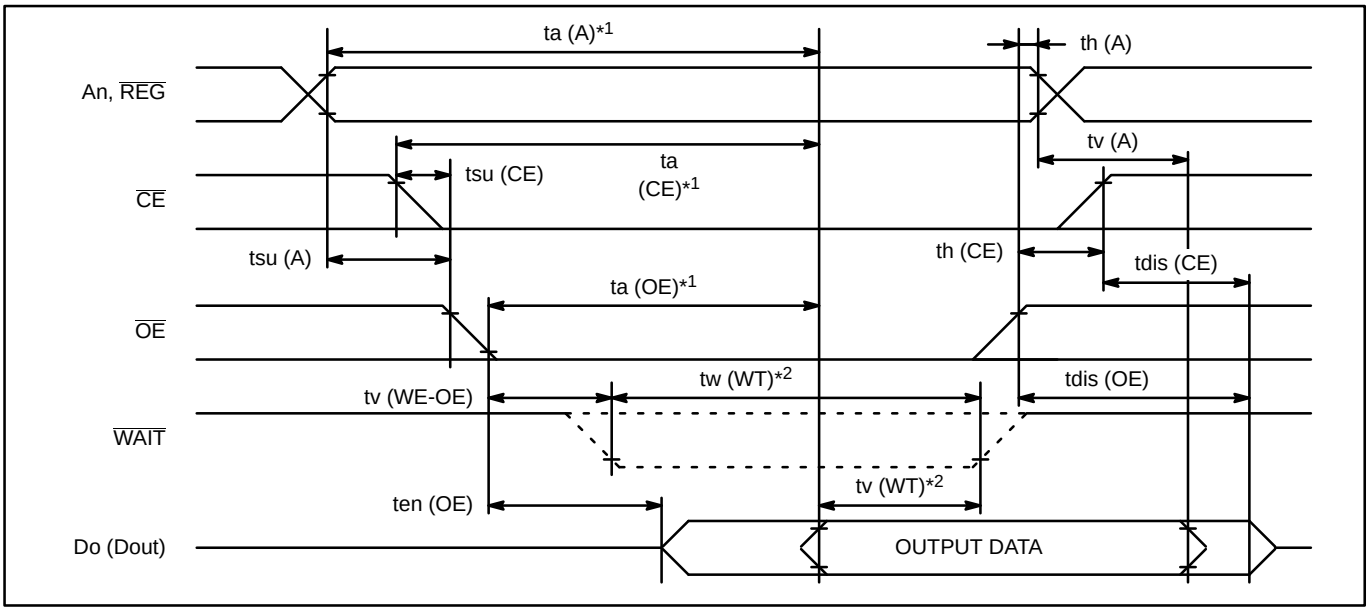
Notes:
1. For card supporting $\overline{WAIT}$
2. When WAIT executed in cycle operation

(2) Read timing diagram



Note: Hatched parts are High/Low. $\overline{WE}$ is High. Output load = 1TTL + 100 pF.

(3) Diagram of WAIT reading time

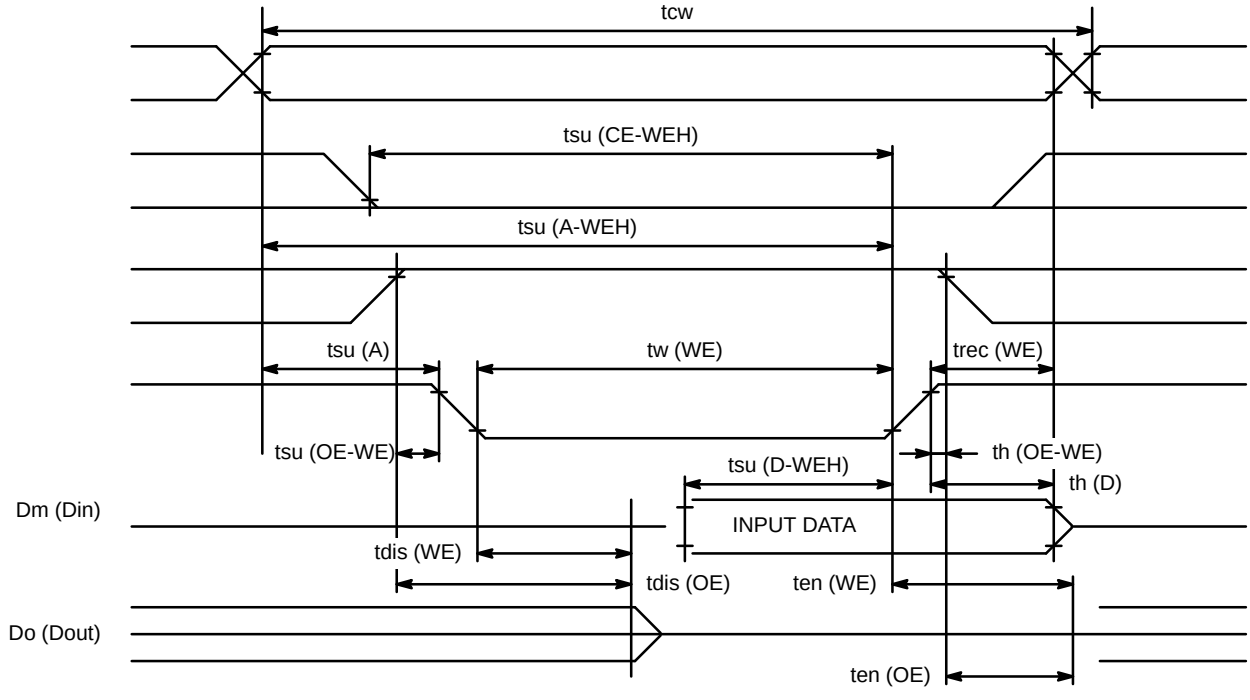


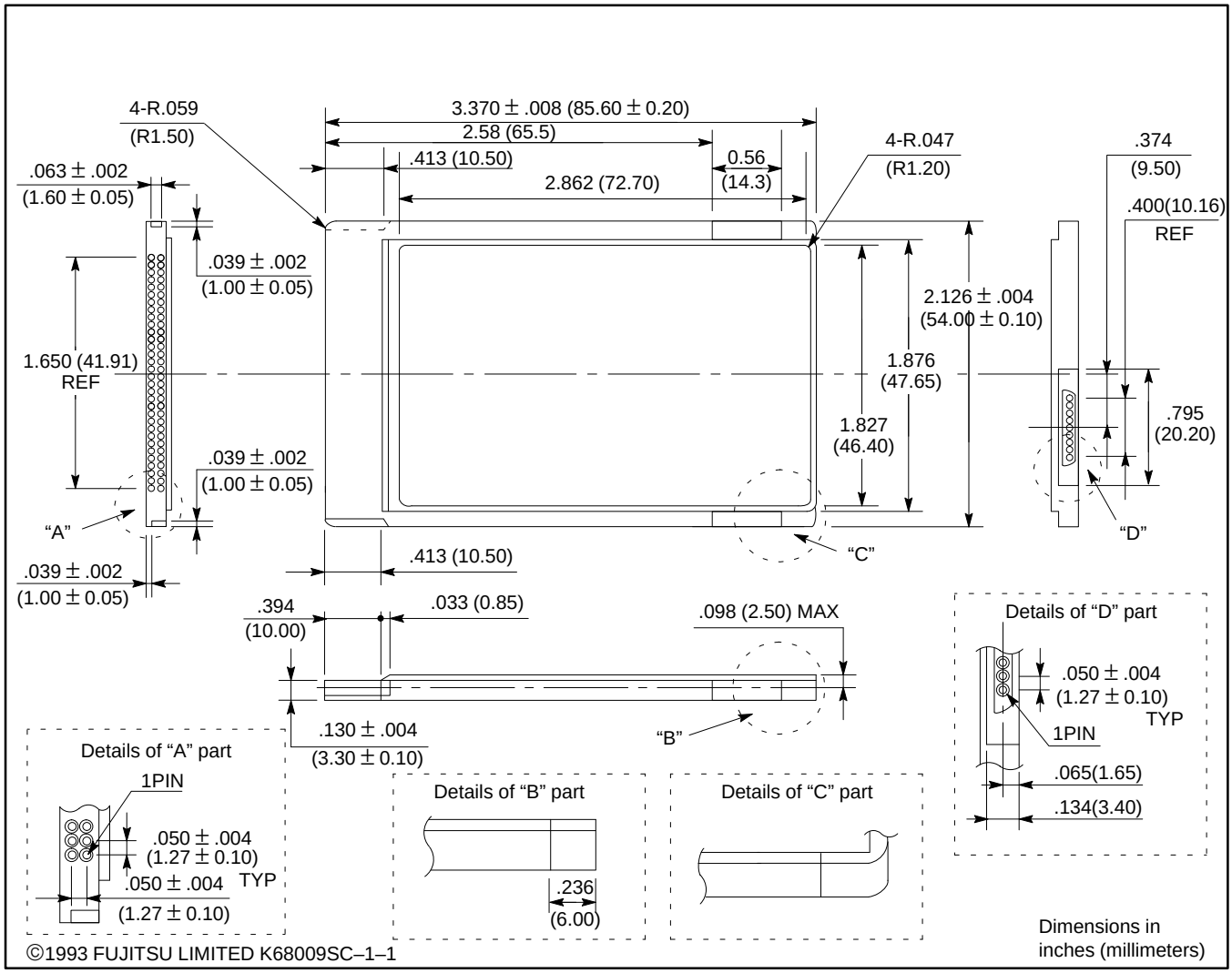
*1 When card wait not output

*2 When card wait output

Note: Hatched parts are High/Low. $\overline{WE}$ is High. Output load = 1TTL + 100 pF.

(4) Write timing diagram (WE control)





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